Bridging the Microwave-to-Photonics Gap with Terahertz Frequency Multipliers

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Forewords

This article on THz frequency multipliers constitutes the core of a French HDR project (habilitation to supervise research). It is mainly based on several previous published journal articles or presentations by the author with several recent inputs submitted for publication. The raw material taken from the publications was assembled and illustrated in more details than in the journal format to form an introduction to the field through the author's particular experience and research. This article will present a brief review of the CW source technologies that are currently available and discuss recent progress and results that has been achieved with THz frequency multipliers.

1. Introduction

Lack of tunable, broadband, robust and reliable power sources in the submillimeter-wave frequency range has been a major limiting factor in developing applications in this part of the spectrum. The range from 0.3 THz, where transistors show only limited gain, to about 10 THz, where solid-state lasers become available, continues to be of significant scientific interest where sources are much needed [1]-[4] (see Fig. 1.1.) Photonic solutions to coherent generation at terahertz frequencies have dominated the field for decades starting with far infrared lasers able to produce tens of milliwatts of coherent power, to femtosecond infrared lasers and photoconductors that enable broadband terahertz sources suited for numerous spectro-imagery applications [5]. Photomixers are also an attractive solution for generating coherent terahertz CW waves thanks to their wide frequency tunability [6], [7]. Recently, quantum cascade lasers have made incursions into the sub-terahertz domain and are routinely delivering milliwatts or tens of milliwatts in the 1 to 4 THz range [8], [9] albeit at cryogenic temperatures and with limited bandwidth. These lasers have been successfully phase-locked and used to build the local oscillator of a heterodyne receiver based on a super-conducting Hot-Electron-Bolometer (HEB) mixer working at 2.8 THz [10].

In contrast, electronic sources in the terahertz region are scarce; if we put aside non solid-state sources like the power-hungry and heavy BWOs that can work to about 1.2 THz, there is indeed only one proven solution: frequency multiplier chains from the microwave region to the terahertz. With current technology terahertz frequency multipliers, power is measured in microwatts rather than milliwatts. The current state of the art at room temperature is 3 μW at 1.9 THz [11], 15-20 μW at 1.5- 1.6 THz [12], [13] and 100 μW at 1.2 THz [14]. As predicted in [15], these powers improve dramatically upon cooling: the same sources produce respectively, 30 μW, 100 μW and 200 μW at 120 K.

Despite relatively low output power levels, frequency-multiplied sources have some decisive advantages that make them the technology of choice for building the local oscillators of heterodyne receivers: firstly, they are inherently phase-lockable and frequency agile, secondly, they work at room temperature, or at moderate cryogenic temperatures for enhance performance; thirdly, multiplier sources are robust enough, compact enough, and use sufficiently low level of DC power to claim several years of heritage in the selective world of space technologies. From AURA [16] to the Herschel Space Observatory [17], frequency multipliers have demonstrated their real-word operability and are proposed for even more challenging missions to the outer planets [18].

The prospect of having a milliwatt-level broadband terahertz frequency-multiplied source would have seemed far fetched just a few years ago. This article will present in section 4 a 0.9 THz frequency tripler that delivers more than 1 mW at room temperature when pumped with a fully solid-state source. This level of power has already enabled the demonstration of an 840-900 GHz fundamental balanced Schottky receiver that exhibits state-of-the-art noise and conversion loss [19]. It can also enhance terahertz imaging applications by driving frequency multipliers to even higher frequencies [20]-[22], such as the 2.5-2.7 THz band.

Considering these new results as well as recent advances in thermal management of frequency multipliers [23], the continuous progress of power amplifiers around or above 0.1 THz [24], and the prospect of high-breakdown-voltage GaN Schottky diodes for submillimeter wave multipliers [25], [26], it is clear that electronic coherent sources have the potential to deliver milliwatts of tunable single-mode power well into the terahertz range.

This article will addresses in section 2 some design techniques before detailing in section 3 the evolution of the technology that culminated with the building of the local oscillators of the Heterodyne Instrument for the Far Infrared on board of the Herschel Space Observatory. Section 4 will present the most recent evolution of the field towards building milliwatt-level tunable electronic sources working at several terahertz.

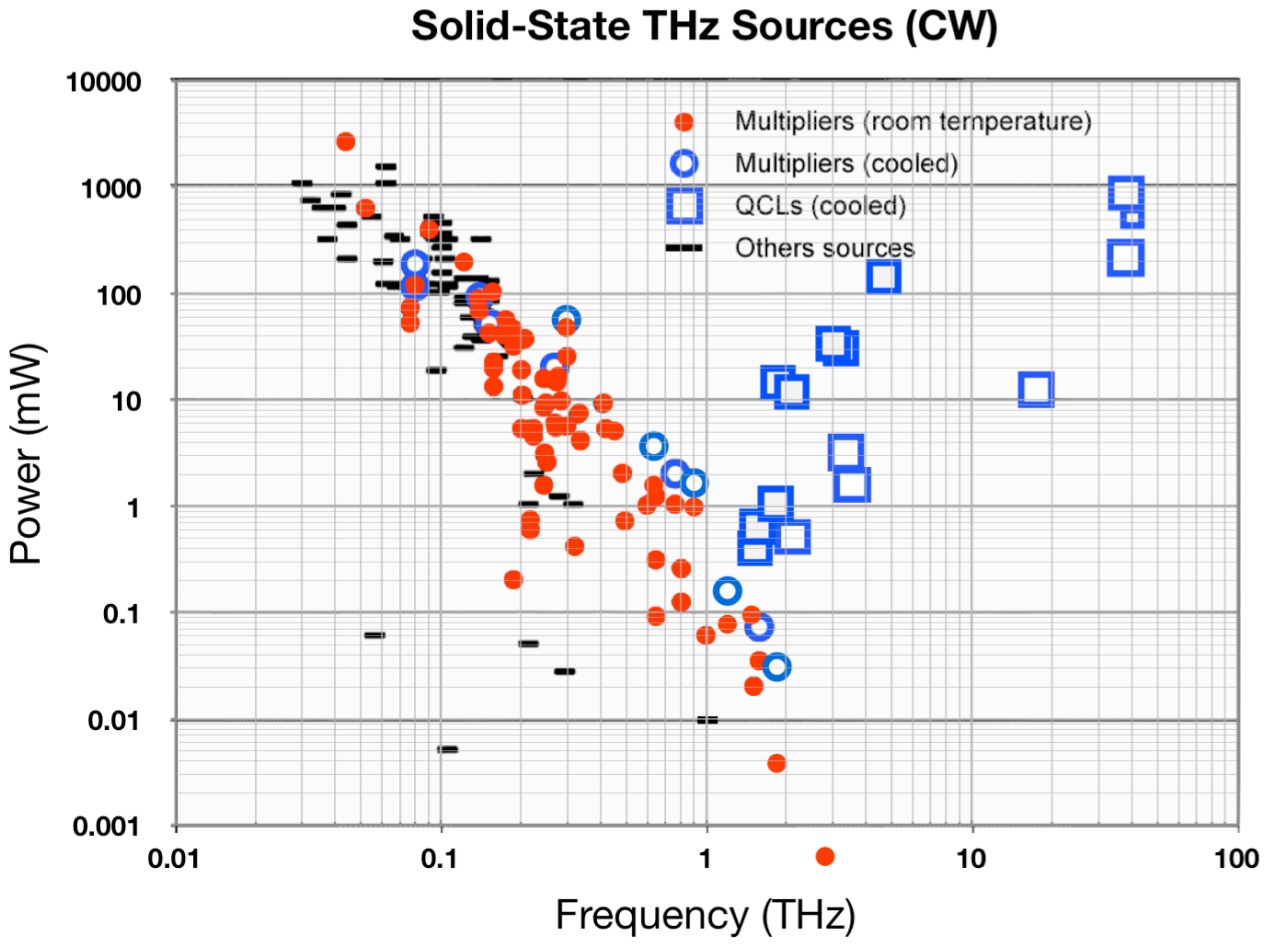


Fig. 1.1. Terahertz gap with respect to source technology. Quantum cascade lasers (□) are progressing downward from higher frequencies, while electronic technology is progressing upward. Frequency multipliers (●) dominate other electronic devices (−) above about 150 GHz. Cryogenic results are shown as hollow symbols. Adapted from T. Crowe, October 2005. New data added by the author, December 2009.

2. A practical approach to the design of frequency multipliers

2.1. Definitions

A frequency multiplier of order N is an electronic device that converts an input sinusoidal signal of frequency F1 and power P1 to an output sinusoidal signal of frequency $F_N=N\times F_1$ and power P_N .

In practice a frequency multiplier generates unwanted harmonics at frequencies $F_k=k\times F_1$ with $k\neq N$ and power P_k with $\sum_{k\neq 1,k\neq N}^{\infty} P_k \ll P_N$ (frequency multipliers). A frequency multiplier is therefore different from a comb generator that generates a series of harmonics which power decreases (usually) with the increasing frequency : $P_k \geq P_{k+1}$ (comb generators). To maximize the power produced at the N^{th} harmonic, one must pay attention to the matching at the output frequency but also to the matching at the idler frequencies. For

instance, a frequency tripler needs to be properly matched at the 2nd harmonic to essentially produce power at the third harmonic. This can be achieved by different means including the use of symmetrical structures to eliminates some unwanted harmonics.

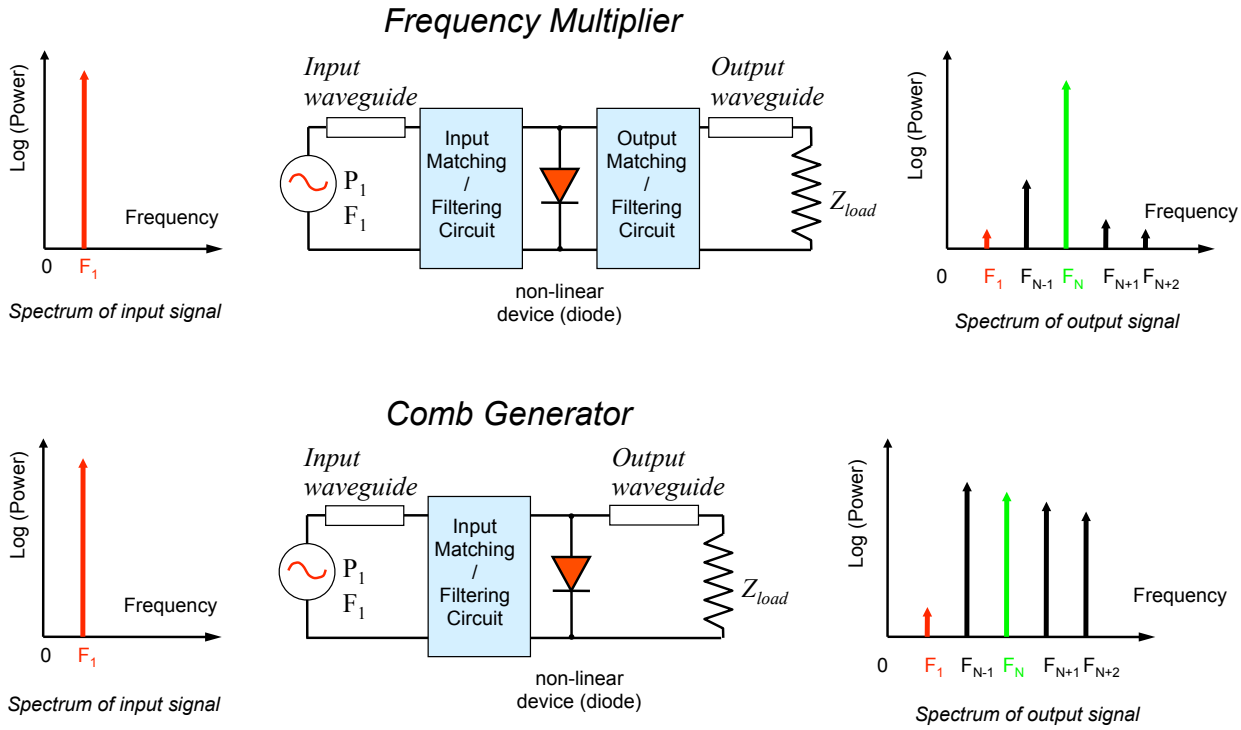


Fig. 2.1. Frequency multiplier vs comb-generator

2.2. Balanced designs: example of multi-anode frequency triplers

Symmetries introduced in the frequency multiplier circuit topology can result in the elimination of even or odd harmonics, hence in an increase of conversion efficiency. This section will describe a particular topology employed in all the state-of-the art sub-millimeter wave frequency triplers presented later in this article.

An efficient topology for submillimeter-wave balanced triplers has been demonstrated in [27]. The topology that was chosen for our frequency triplers adopted a configuration used in [28] at millimeter wavelengths. It as the advantage of allowing four or more anodes per chip, dramatically increasing power handling capabilities and consequently the output power.

The triplers use a split-block waveguide design and feature two to six Schottky planar varactor diodes, monolithically fabricated on a GaAs-based substrate (see Fig. 2.2). The diodes are connected in series at DC and are in a balanced configuration at RF, due to the symmetry of the circuit (details are given in the following section). The chip is inserted between the input and the output waveguides in a channel. An E-plane probe located in the input waveguide couples the signal at the fundamental frequency to a suspended microstrip line that can propagate only a quasi-TEM or, in one case, a true TEM mode. This line has several sections of low and high impedance used to match the diodes at the input and output frequency and to prevent the third harmonic from leaking into the input waveguide. The third harmonic produced by the diodes is coupled to the output waveguide by a second E-plane probe. The circuit features additional matching elements in the input and output waveguides, made with a succession of waveguide sections of different heights and lengths.

To increase the spectral purity of the frequency tripler, the dimensions of the output waveguide has been chosen to cutoff any second harmonic leakage that could result of a circuit unbalance. In addition, the balanced geometry of the circuits ensures that power at the fourth harmonic of the input is strongly suppressed. The closest harmonic that can leak is the fifth, but, given the fact that the capacitance of the diodes are optimized for the third harmonic, no significant power is expected at the fifth harmonic.

Thanks to this topology, the bias scheme is very simple. It consists of an on-chip capacitor at one end of the series of diodes near a narrow aperture in the wall of the chip channel. Extensive simulations were done to confirm that the bias circuit has almost no impact at RF frequencies.

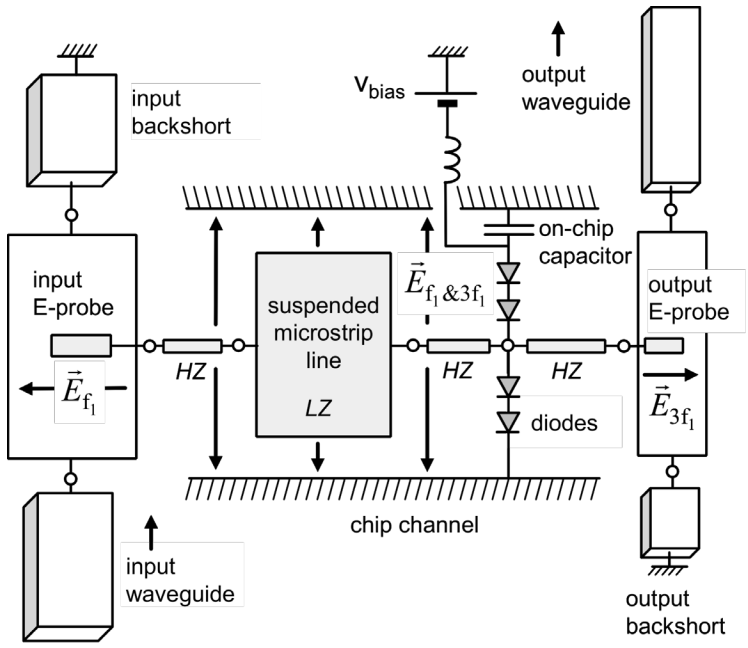
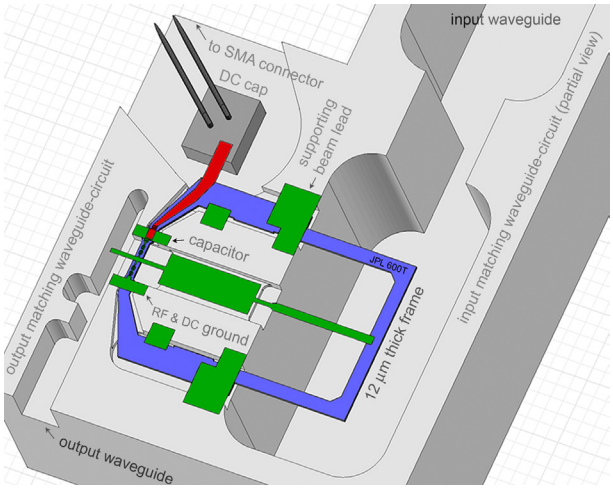
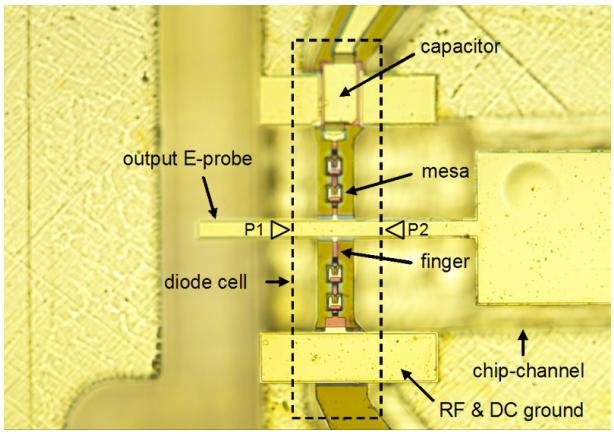


Fig. 2.2. Block diagram of a 4-anode balanced tripler. Additional waveguide sections of different impedances and lengths (not shown) are used for the input and output matching. HZ and LZ stand respectively for high and low impedance. $\vec{E}_{f_1}$,$\vec{E}_{3f_1}$ and $\vec{E}_{f_1\&3f_1}$ stand respectively for the electric field at the fundamental frequency f_1, at the output frequency $3f_1$, and both at the input and output frequency.

The chip is suspended above the bottom half of the channel by gold beam leads spaced around the substrate. Two of these beam leads provide the required DC and RF connections for the diodes when clamped between the two halves of the split block. Fig. 2.3a show the structure of a 4-anode frequency tripler designed to work in the 540-640 GHz band, while Fig. 2.3b shows details of the diode area.



(a)



(b)

Fig. 2.3. (a) : 3D view of the bottom part of the waveguide block with the four-anode 600 GHz tripler chip and the DC capacitor (design by the author). The top part of the waveguide block (not shown) is symmetrical. The complete input matching waveguide-circuit (cutoff in the figures) consists of several reduced-height and standard-height rectangular waveguide sections. This tripler was used as the second stage driver of the 1.6-1.7 THz and the 1.7-1.9 THz local oscillator of the heterodyne instrument on the Herschel Space Observatory. (b) : Detail of a 4-anode 600 GHz tripler chip showing the anodes, the on-chip capacitor, the output E-probe and

part of the on-chip matching circuit. The dashed line rectangle defines the diode cell used for the first step of optimization. P1 and P2 define the localization of the HFSS wave ports used in the simulations (see section 2.4).

2.3. Necessary condition to balance the circuit

The topology of this type of frequency tripler provides adequate symmetry for a balanced design, but there is an additional condition that the circuit must satisfy. In this design, the input signal at the fundamental frequency $f_1 = \omega_1 / 2\pi$ and period $T_1 = 1 / f_1$ propagates along the suspended microstrip line on a quasi or pure TEM mode and creates, in the vicinity of the diodes, an excitation field $\vec{E}_1(\omega_1 t)$ that generates the currents $i_a(t)$ and $i_b(t)$ in the diodes (see Fig. 2.4). If the asymmetries of the design are small enough, due to the orientation of the diodes, the relation between $i_a(t)$ and $i_b(t)$ is given by:

$$i_b(t) = i_a(t + T_1 / 2) \qquad 1) \quad ($$

As shown in [29], equation (1) can be used to write $i_a(t)$ and $i_b(t)$ as

$$i_a(t) = \sum_{n=-\infty}^{n=+\infty} a_n \cdot e^{jn\omega_1 t} \qquad (2)$$

$$i_a(t) = \sum_{n=-\infty}^{n=+\infty} a_n \cdot e^{jn\omega_1 (t+T_1/2)} \qquad (3)$$

where $(a_n)_{n\in\mathbb{Z}}$ are complex coefficients that depend on the circuit and the strength of the fundamental signal. With the following notations:

$$I_{even\ H} = \sum_{n=-\infty}^{n=+\infty} a_{2n} \cdot e^{j2n\omega_1 t} \qquad (4)$$

$$I_{odd\ H} = \sum_{n=-\infty}^{n=+\infty} a_{2n+1} \cdot e^{j(2n+1)\omega_1 t} \qquad (5)$$

equations (2) and (3) become:

$$i_a(t) = I_{even\ H} + I_{odd\ H} \qquad (6)$$

$$i_b(t) = I_{even\ H} - I_{odd\ H} \qquad (7)$$

The currents $I_{even\ H}$ and $I_{odd\ H}$ contain respectively the currents at the second and the third harmonics. They are new sources that generate electromagnetic waves in the circuit. Because of the symmetry, the currents $I_{even\ H}$ generate two sets of electromagnetic waves flowing in opposite directions and defined respectively by the electric fields $\vec{E}^{-}_{even\ H}$ and the currents $i^{-}_{even\ H}$ and by the electric fields $\vec{E}^{+}_{even\ H}$ and the currents $i^{+}_{even\ H}$. Both currents, $i^{-}_{even\ H}$ and $i^{+}_{even\ H}$, consist of two components of the same magnitude but opposite sign flowing along the edges of the suspended microstrip line. On the other hand, the currents $I_{odd\ H}$ generate two sets of electromagnetic waves flowing in opposite directions and are defined respectively by the electric fields $\vec{E}^{-}_{odd\ H}$ and the currents $i^{-}_{odd\ H}$ and by the electric fields $\vec{E}^{+}_{odd\ H}$ and the currents $i^{+}_{odd\ H}$. Both the currents $i^{-}_{odd\ H}$ and $i^{+}_{odd\ H}$ are divided into two components of the same magnitude and sign, flowing along the edges and the center of the suspended microstrip line. Consequently, if the dimensions of the circuit allow it, the electromagnetic waves generated by the currents $I_{even\ H}$ propagate in a TE mode along

the suspended microstrip line, whereas the electromagnetic waves generated by the currents $I_{odd\ H}$ propagate in a TEM mode, independently of the circuit dimensions. Therefore, to balance the circuit it is important to confine the second harmonic in a virtual loop, and the TE mode should be cut off at the idler frequency.

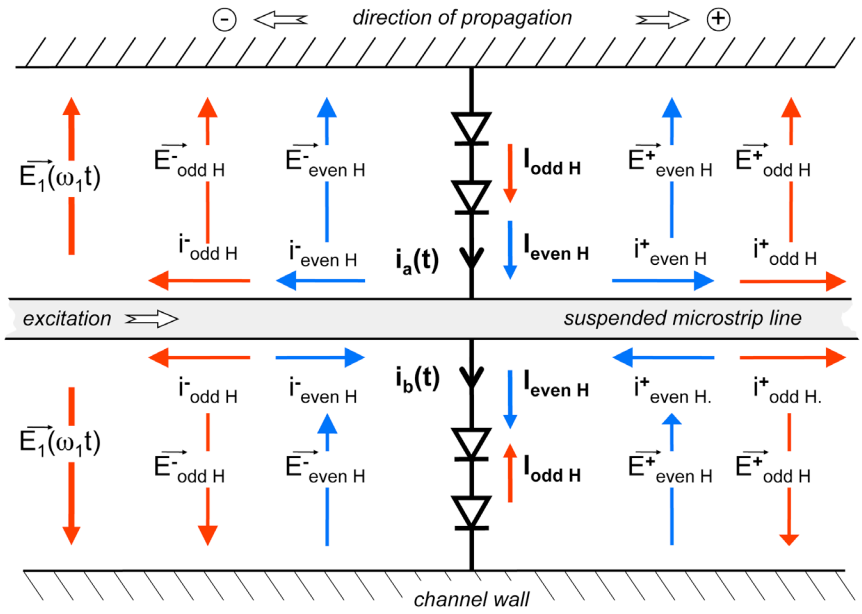


Fig. 2.4. Currents and electrical fields in the vicinity of the diodes. The DC bias circuit is not represented to simplify the interpretation. The designations "even H" and "odd H" refer respectively to even harmonics and odd harmonics.

1. Design optimization

This section will present a practical methodology that was used to design several wide-band, fix-tuned, state-of-the-art frequency triplers in the 0.3 THz to 2 THz range. While a number of concepts defined in [30] for balanced doublers are utilized, a number of significant points must be addressed for the the balanced triplers presented in this article.

Usually, the first step in the design of a frequency multiplier is to determine the characteristics of the diodes along with the operating conditions that best suit the application. In this case, it consists of optimizing the doping level, the anode dimensions, and the bias voltage for a given input power. Once these parameters are fixed and the optimum embedding impedances of the diodes are determined, a linear circuit can be synthesized [31].

For the design of our triplers, the chip topology as well as the diode characteristics are iteratively modified till a suitable compromise is achieved between the efficiency and bandwidth. Commercially available harmonic balance software codes are used to carry out the optimization. During this design process it is important to make sure that coupling balance between the anodes is preserved and realistic circuit losses are accounted for. Contrary to the balanced doublers proposed in [32], both the input and the output signals propagate with the same mode in the region immediately around the diodes. Therefore a filter is required and it can be optimized more easily using the non-linear simulations.

i) Non-linear modeling of the Schottky diode.

Abundant literature is available about the modeling of Schottky diodes at millimeter and submillimeter wavelengths working at room temperature [33]–[38] and at cryogenic temperatures [39]. For all our designs, we use a simplified electrical model, consisting of a nonlinear junction capacitance C_j in parallel with a nonlinear conductance G_j and in series with a resistance R_s.

a) For varactor Schottky diodes, the junction capacitance is classically modeled as follows [40]:

$$\text{For } V \le \frac{V_j}{2},\ C_j(V) = \frac{A\varepsilon_s}{t(V)} \qquad (8)$$

Where $t(V) = \sqrt{\frac{2\varepsilon_s}{qN_D} \cdot \left(V_j - V\right)}$ *(9)*

For $V \geq V_j/2$, $C_j(V)$ is defined by a linear extrapolation of equation (8) from $V=V_j/2$, to avoid the singularity of equation (8) at $V=V_j$. V is the bias voltage, V_j the built-in potential, ε_s the semiconductor electric permittivity, A the junction area, t(V) the thickness of the depletion layer, q the charge of the electron, and N_D the doping of the semiconductor epilayer. For the GaAs Schottky diodes fabricated at JPL, V_j is approximately 0.85 V at room temperature.

As the anodes get smaller and smaller, a correction term should be added to Cj(V) to take into account the edge effects. This term has two components: a first order term that is not modulated, and a second order term that is modulated [35]. The correction terms given in [35] apply to circular anodes and are a function of the anode radius. As the multipliers fabricated at JPL use rectangular anodes, we modified the correction term to be a function of their length and width. We only kept the first order correction term that corresponds to a linear capacitance in parallel to the nonlinear plate capacitance of the junction; the other term was find to be negligible for anodes of a few μm^2.

b) The nonlinear conductance is derived from the classic equations of thermionic emission in Schottky contacts [40].

Saturation effects [33]–[35] and breakdown effects are not directly included in the simulation. However, time domain simulations are performed to check that the voltage across the diodes never enters breakdown to minimize the risk of damaging the diodes [41].

The value of the reverse saturation current I_{sat} influences significantly the predicted performance, especially when the input power is high enough to create a direct current through the diodes. Its value depends strongly on the actual temperature of the junction, which is difficult both to measure and to predict. Therefore, some uncertainty is introduced by this parameter into the model.

c) The series resistance Rs of the planar diode affects the efficiency of the multiplier. Significantly underestimating the value of Rs affects the optimization of the design itself: the optimized junction capacitances would be too big and the bias voltage too far in the reverse regime. With respect to the predictions, the actual multiplier performance would be degraded and shifted down in frequency. To partially compensate for the frequency shift, one would have to use devices with smaller anodes.

DC measurements of Rs give an indication of the quality of the diodes, but the measured values are usually too low to be used in the RF simulations. On the other hand, calculations of the series resistance have to take into account the particular topology of the planar diode, where skin effects play a major role. In addition, any physical model of the Schottky barrier has to be properly implemented in a circuit simulator, unless only linear impedances of the diodes are used. Our approach relies on the empirical rule introduced in [42] that consists in fixing the product Rs×Cj(0). This value is derived empirically. For submillimeter wave multipliers working at room temperature and for a doping of $1 \cdot 10^{17}$ cm^{-3}, Rs is set to :

$Rs \times Cj(0) = 120\ \Omega \times fF$ *(10)*

For the 4-anode 600GHz frequency tripler presented above, this rule gives Rs ≈ 20 Ω per diode compared to the DC measured value of Rs=8 Ω per diode. Note that for multipliers working at higher frequencies and for higher doping levels, a lower value of the product Rs×Cj(0) is used.

ii) 3D modeling of the diodes.

The electromagnetic field around the diode is calculated with Ansys HFSS and is measured with a virtual probe, placed at the location of the Schottky contact. This probe is defined as an internal wave-port in HFSS (see Fig. 2.5a). The anode itself defines the inner conductor; the outer conductor is defined by the edges of a small rectangle that lies on the top face of the mesa around the anode (thus the probe has no length). The gap between the edges of the anode and this rectangle has to be very narrow to avoid underestimating the parasitic capacitance. The definition of the port and the meshing around the diode are critical to get accurate results. The 3D geometrical structure of the diode must also be drawn accurately. Details such as the passivation layers greatly contribute to the parasitic capacitances and must be included in any accurate 3D representation of the diode.

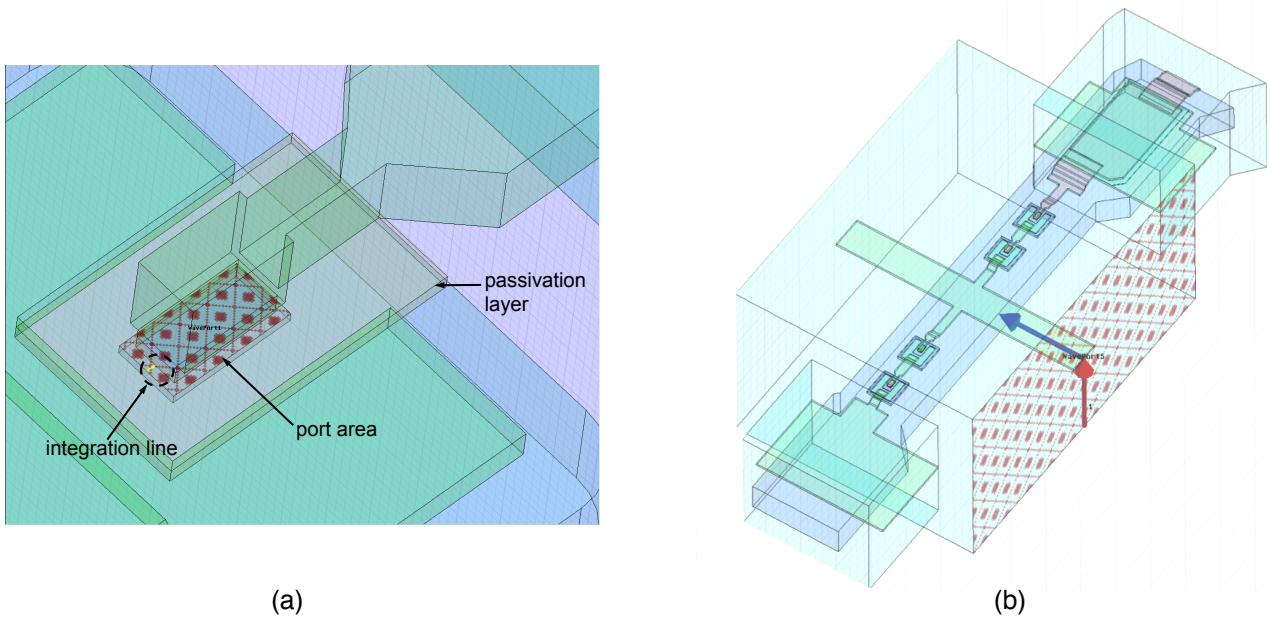


Fig. 2.5. (a) : Definition of the HFSS wave-port at the exact location of the Schottky contact. The integration line defines the polarity of the diode. (b) : HFSS model of the diode cell and definition of port P2.

iii) Modeling of the diode cell

For triplers, the second harmonic idler plays an essential role in the transfer of energy from the fundamental to the third harmonic [43]. Therefore, the diodes need to be properly matched at the idler frequency. Indeed, their embedding impedances should be as close as possible to pure reactances. To greatly facilitate the synthesis of such impedances, the circuit has to be balanced. This requires that the diode cell satisfy the conditions mentioned above. In addition, the capacitance of each diode needs to be compensated by adjusting the length and the width of the fingers, the size of the mesas and the dimensions of the cross-section of the chip-channel (see Fig. 2.4 and Fig. 2.7). Diodes with small junction capacitance require longer fingers (implying wider channels) or higher channels than diodes with large junction capacitances.

An initial diode cell is drawn based on the chip topology. Its S-parameters are first calculated with Ansys HFSS and then used in harmonic-balance simulations to determine which junction capacitance and bias voltage give the maximum output power. It is important to take into account the ohmic and dielectric losses of the circuit in all the simulations. The balance between the diodes is monitored for all the relevant frequencies. We used Agilent ADS suite for these calculations.

The diode cell alone cannot be an efficient tripler; thus, harmonic-dependant complex impedances are connected to the ports of the ADS simulation bench that correspond to the HFSS wave-ports P1 and P2 (see Fig. 2.3b and Fig. 2.5b). These ports excite only a quasi or a pure TEM mode of the suspended microstrip line. The complex impedances are optimized for the center of the band. The output power is calculated at either port P1 or port P2. To have some idea of the instantaneous bandwidth, the frequency is swept across the band. Then, the 3D-stucture is modified according to these results and the rules mentioned earlier in this paragraph. Many iterations are often required to converge to a satisfactory solution.

iv) Input and output matching circuits.

Once the diode cell and the size of the anodes are fixed, the different sections of the suspended-microstrip line and the input and output E-probes are optimized to maximize the conversion efficiency and the input coupling. The design is driven by the necessity to minimize the number of on-chip matching elements in order to reduce both the chip dimensions and the losses. At this stage of the design, most of the multiplier is already in place and a fine-tuning of the diode cell and anode size is performed. Upon completion of this step, the chip topology is fixed.

To extend the bandwidth, we add to the input waveguide a succession of sections of high and low impedance. As they have no impact on the output match, it is possible to use only linear simulations. To broaden the output match, the same method is applied to the output waveguide.

3. Technology of frequency multipliers and the Herschel Space Observatory

This section give a brief history of the tremendous technological improvements that made possible the building of the local oscillators of the Heterodyne Instrument for the Far Infrared onboard of Herschel Space Observatory. Herschel has the largest mirror to have ever flown in space with a diameter of 3.5 m working up to 5.5 THz (55 µm of wavelength).

3.1. From Whisker-contacted diodes to Planar Discrete Diodes

Frequency multipliers using whisker-contacted Schottky diodes played an important role in the development of heterodyne receivers for radio astronomy and planetary sciences. As predicted by Räisänen in 1992, they appeared to be the only available solution for the LOs of space-borne submillimeter-wave heterodyne instruments in the years 1995-2000. Actually, ODIN, launched on February 2001, was the first satellite to embark heterodyne receivers in the 486-580 GHz band using whisker-contacted Schottky multipliers as final stages of the LOs [44]. But in 1992 this already mature technology was still unable to pass the 1 THz mile stone [45]. Progress toward the terahertz region was reported by Crowe and Rüdiger Zimmerman in 1996 [46] before Peter Zimmerman reached 1.135 THz in 1998 with an all-solid-state source that produced 40 µW of output power [47]. The Schottky diode was usually mounted in a crossed-waveguide structure featuring several mechanical tuners. The input and output signals were decoupled through a low-pass filter, which was either coaxial (Räisänen / Erickson's design) or a stripline structure (Takada / Archer's design) —see ref. [45]. At submillimeter wavelengths and until the year 2000, whisker-contacted diodes outperformed Schottky planar diodes introduced in the mid-eighties by Cronin and Law [48] at the University of Bath, UK, and shortly later by Bishop and Mattauch [49] at the University of Virginia (UVa), USA, due to their lower parasitic capacitances and lower series resistances. However, at millimeter-wavelengths Schottky planar discrete diodes started to give better performance due to the use of multiple-anodes in balanced configurations. Erickson's balanced doublers, proposed and demonstrated in [50]–[52], have become a standard topology for frequency multiplication due to their good performance. This topology was used recently by Porterfield in a 0.65 W-pulsed power 190 GHz balanced doubler featuring no less than 18 anodes [53].

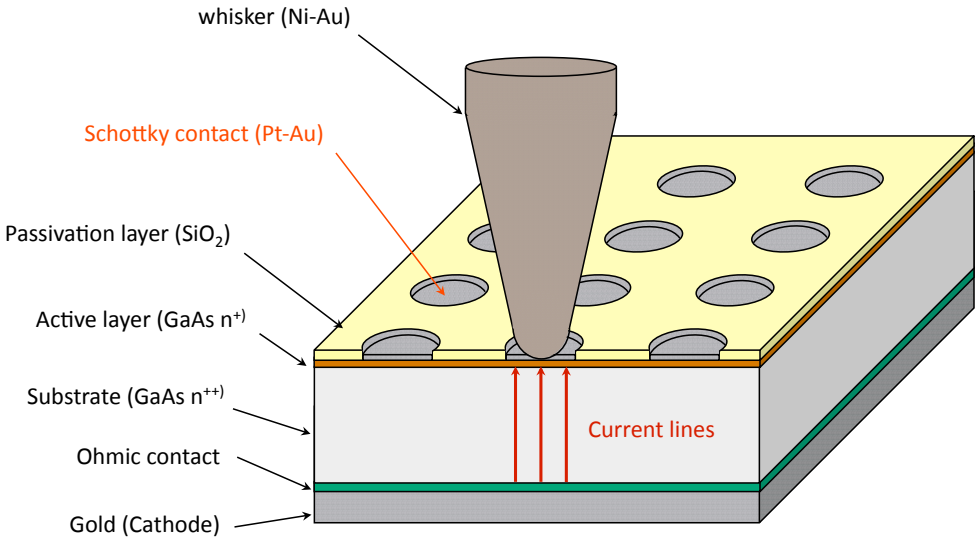


Fig. 3.1 Schematic of a whisker-contacted Schottky diode

In the nineties, GaAs-based Heterostructure barrier varactors (HBV) were introduced by Kollberg and Rydberg at the University of Chalmers [54], Sweden, as alternate diodes. They were initially made to be whisker-contacted before being made planar. HBV diodes produce only odd harmonics of an incident signal due to their internal symmetry. Thus, they are attractive devices to design high order odd harmonic multipliers such as triplers [55], [56] or quintuplers that can reach conversion efficiencies up to 5% at 210 GHz [57] or 11% at 100 GHz [58]. HBV technology took a significant turn in the late nineties when Lippens and Mélique at IEMN, France, introduced InP-based multiple-barrier devices [55]. The results obtained on a 250 GHz waveguide tripler (11% efficiency and 9.5mW of output power) demonstrated that HBV technology was a serious challenger to the classic and simpler Schottky technology. However, despite further efforts by IEMN, Chalmers and UVa, HBV multipliers did not reach the level of performance of Schottky multipliers. Another technique to build devices that exhibit internal symmetries was recently explored by Krach in [59]. It gave a state-of-the-art conversion efficiency of 22% for a 230 GHz planar diode tripler.

3.2. Semi-monolithic frequency multipliers at THz frequencies

In the mid-nineties the release of powerful commercial three-dimensional (3D) field-solvers (Ansoft-now-Ansys HFSS) and non-linear circuit simulators (HP-now-Agilent MDS-now-ADS) transformed the way frequency multipliers were designed and built. These codes greatly increased the accuracy and the speed of the calculations necessary to optimize frequency multipliers. Erickson and Tiovunen pioneered the way by designing a 4-anode balanced doubler at 170 GHz entirely with HFSS and MDS [30]. In this article, they gave rationale to justify the use of 3D field-solvers instead of traditional RF measurements performed on scaled-models: "*Conventional scale model measurements, because of the wide range of sizes (>1000:1), are difficult when one considers the smallest important features on the diode relative to the size of a waveguide mount. Another major problem is providing the small coaxial probes to the diode locations…The advantages of numerical analysis are that one may easily study dielectric thickness effects, optimum inductances in the diode package, power balance between the diodes, and the origin of the parasitic effects.*" Erickson's and Tiovunen's design methodology was rapidly adopted by other researchers and opened the way, several years later, to the design of highly integrated fixed-tuned waveguide multipliers working well above 1 THz.

Within the years 1995-2000, it became clear that discrete planar diodes were limited in frequency due to their size and the difficulty to connect them to the circuit with sufficient precision. Their integration on a circuit featuring several matching elements and providing precise connections to the waveguide block was necessary. However, MMIC-like submillimeter-wave circuits on GaAs substrate presented the inconvenient of being lossy and dispersive due to the high dielectric constant of GaAs (or InP for IEMN HBV diodes). To solve this difficulty several device fabrication technologies were proposed. One consists of transferring the epilayer on quartz (or some other application-optimized substrate) to decrease the losses and dispersion [59], [60], or on high thermal conductivity substrates to address heat dissipation issues [23], [53], [61]. An alternative approach introduced by Mehdi and Smith at the Jet Propulsion Laboratory (JPL), USA, is to decrease dielectric loading by removing most of the substrate from the chip [62]-[65] or by using GaAs membrane technology [11]-[14], [65]-[68]. The first solution, called substrateless technology is used at JPL for sub-THz circuits with substrate thickness ranging from 12 µm to 50 µm depending on the frequency (see Fig. 3.2). For THz circuits, only the membrane process combined with e-beam lithography is used. JPL membranes are 3 µm thick and can be made with no supporting frame (see Fig. 3.3 and Fig. 3.4). The introduction of beam leads (metal membranes) to facilitate chip handling and placement and provide more precise RF and DC grounding brought significant further improvement to this technology [11]-[14], [62]-[68]. It is important to mention that the precision of the machining of the waveguide blocks plays a fundamental role in the working of THz frequency multipliers. For instance, JPL 1.9 THz tripler chips are inserted in a channel which width and depth are respectively 38 µm and 12 µm. The required precision for the alignment of the chip in the channel or the alignment of the two halves of the block is 2-to-3 µm.

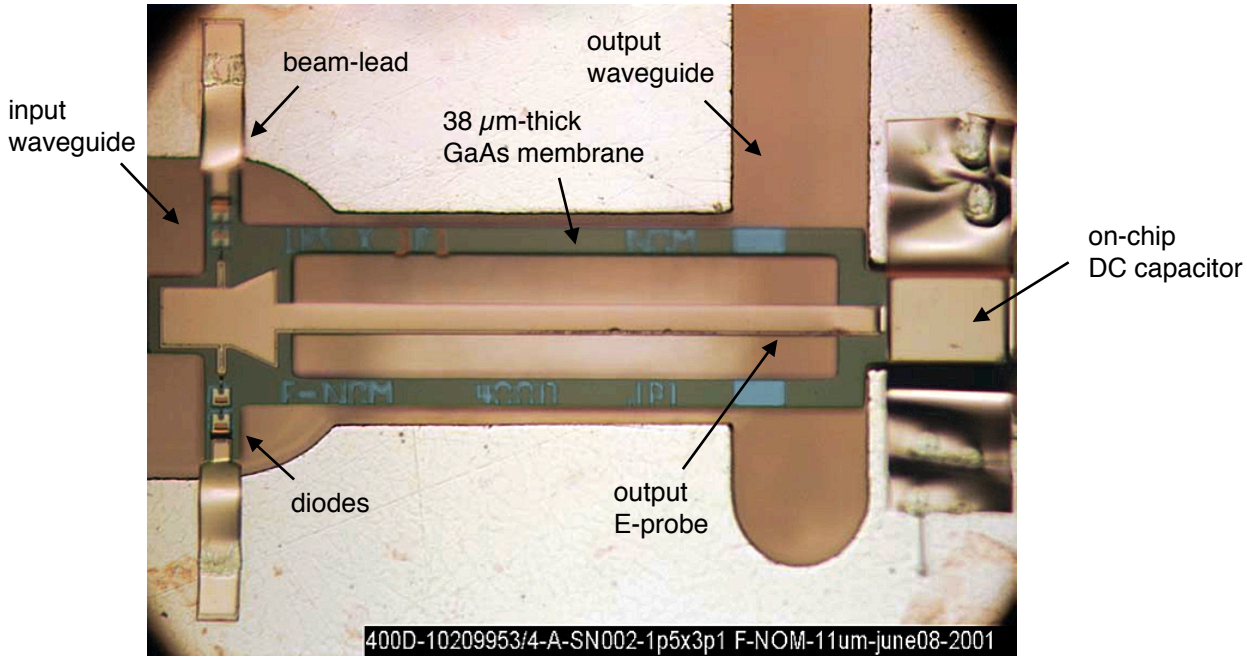


Fig. 3.2: JPL 400 GHz 4-anode doubler with substrate-less technology (design by Erich Schlecht). This Doubler was used as a second stage driver to build the 1.2 THz channel of the heterodyne instrument of the Herschel Space Observatory.

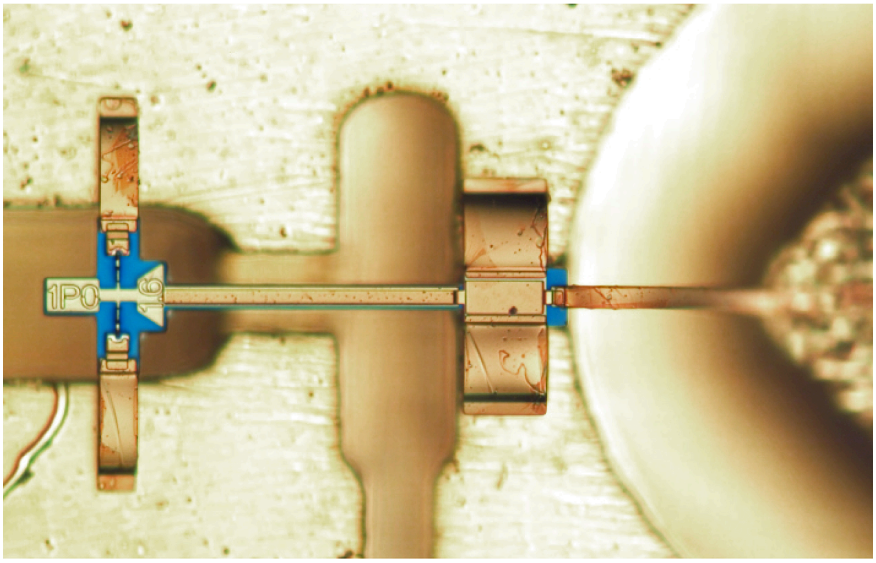
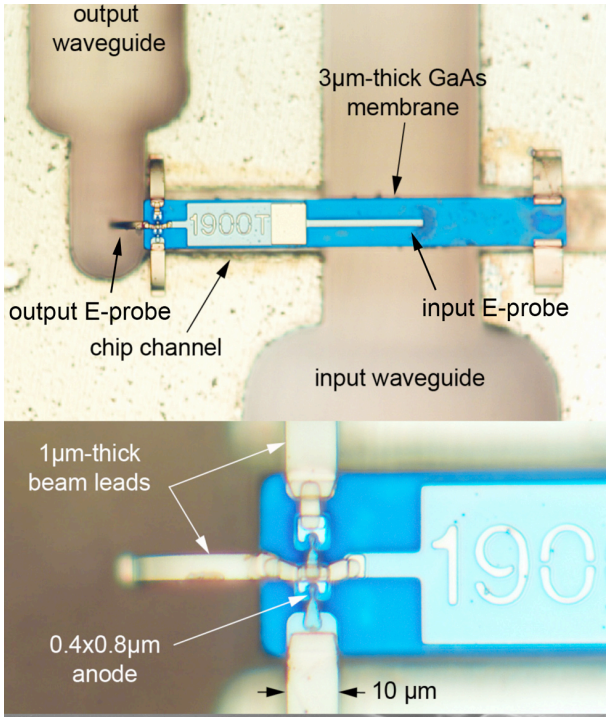
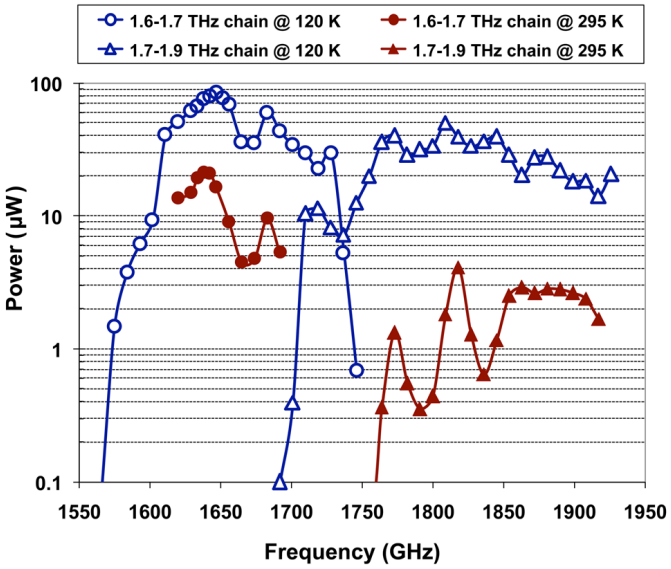


Fig. 3.3: JPL 1500 GHz doubler with JPL frame-less membrane technology (design by Goutam Chattopadhyay). This Doubler was used to build the 1.5 THz channel of the heterodyne instrument of the Herschel Space Observatory.

3.3. THz local oscillators for the Herschel Space Observatory

One of the greatest challenges for the Herschel mission was achieving 10% electronically tunable sources in the 1.6 to 1.9 THz range with sufficient power to each pump a pair of Hot Electron Bolometer (HEB) mixers, which translates to being able to produce more than about 2 μW of output power. Due to the great improvement of the performances of frequency multiplier upon cooling, a passive cooling scheme was implanted in the LO unit to bring the multipliers at an ambient temperature of 120-150K. The W-band power amplifiers used in the chain were left at about 290 K and were separated from the multipliers by 5 cm stainless-steel piece of rectangular waveguide (see Fig. 3.5).





(a) (b)

Fig. 3.4. (a): Last stage frequency tripler used for the 1.6-1.7 THz and 1.7-1.9 THz local oscillator chains of the heterodyne instrument of the Herschel Space Observatory (designs by the author). The top picture shows the chip placed inside the waveguide block. The bottom pictures show a close-up of the chip. (b) : Performance of 1.6-1.7 THz (circles) and 1.7-1.9 THz (triangles) local oscillator chains developed for the heterodyne instrument of the Herschel Space Observatory at room temperature (filled markers) and at cryogenic temperature (open markers).

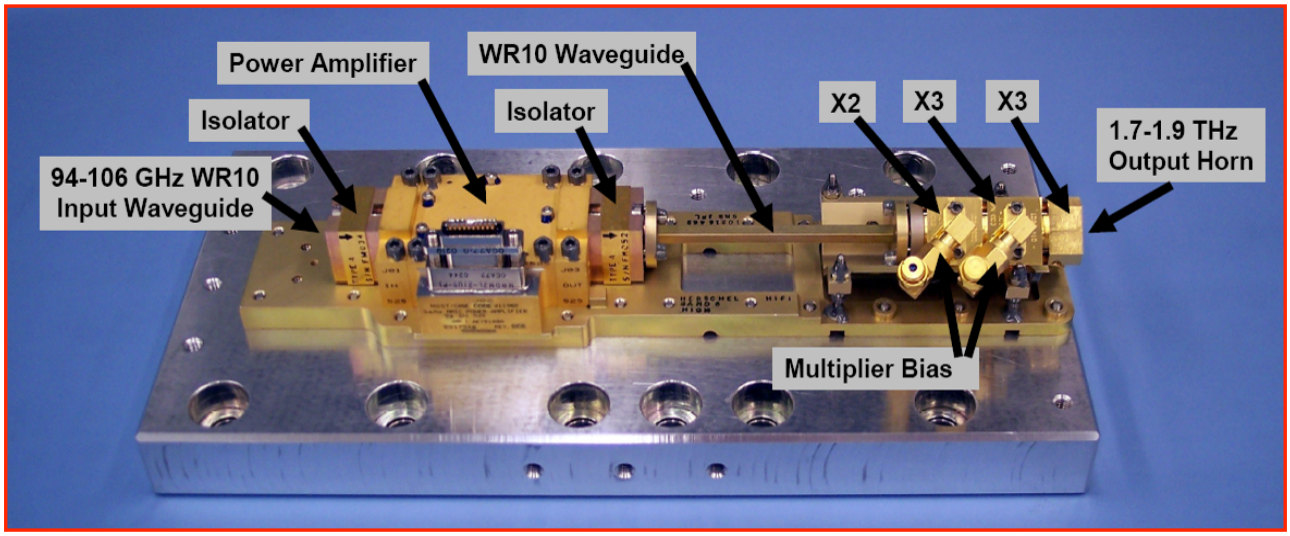


Fig. 3.5: JPL flight model of the 1.7-1.9THz local oscillator chain for HIFI-Herschel.

A ×2×3×3 multiplication scheme was envisioned to cover the desired band in two sub-bands, 1.6-1.7 THz and 1.7-1.9 THz. These multipliers are waveguide biasless balanced frequency triplers featuring two Schottky diodes on a several micrometer thick GaAs membrane (see Fig. 3.4a). They use the same device, except for the size of the anodes (around 0.25 μm^2 of surface area and 1 fF of intrinsic zero bias capacitance per anode). However, the waveguide input and output matching networks are optimized for each sub-band therefore two different waveguide blocks are necessary.

Fig. 3.4b shows the output power produced by the two chains at room temperature and at 120 K. Cooling the chain produces an appreciable increase of bandwidth and output power. There is a three-fold reason for this drastic improvement. Firstly, as the device is cooled the GaAs mobility improves thus improving the intrinsic performance of each diode. Secondly, ohmic losses associated with the waveguides and the on-chip

matching circuits decrease due to the decrease in phonon scattering. Thirdly, as the drive power increases, the efficiency of the last stage increases significantly since, at room temperature, the last stage is under-pumped. The 1.6-1.7 THz chain produced a record room-temperature output power of 21 μW and an estimated conversion efficiency of 1.5% at 1647 GHz. A record output power of 86 μW with an estimated efficiency of 3% was measured at 1647 GHz at 120 K.

The 1.7-1.9 THz chain produced an output power of 4 μW at room temperature with an estimated efficiency of 0.4% at around 1818 GHz. At 120 K, the measured peak power was 50 μW around 1809 GHz and the estimated efficiency was 1%.

It must be point out that these results far exceeded expectations. Until december 2002, when the first tests of the 1.9 THz tripler were performed, it was unclear if the 1.9 THz channel would ever be able to provide the required 2 μW of power to pump the HEB mixers. Instead, the peak power reached on the 1.6-1.7 THz and 1.7-1.9THz channels exceeded the needs by a factor 50 and 15 respectively! Nearly six years after having been obtained, these results still constitute the state-of-the art of the field.

4. Increasing power handling capabilities

The practical limit of the output power of a frequency multiplier is typically either the power beyond which conversion efficiency drops off due to saturation effects or the device lifetime becoming unacceptably short due to thermal or reverse-breakdown effects [41]. To increase power handling, the device doping can be optimized and the number of anodes per chip can be increased. Additionally, the epilayer can be transferred to a high thermal conductivity substrate [23], [53], [61]. While multi-anode frequency doublers have been widely studied in the past [30], [51]-[53], [62], [63] frequency triplers with more than two anodes have been demonstrated only recently. For example, wideband and high efficiency balanced triplers at 300 GHz and 600 GHz featuring respectively six and four Schottky anodes per chip have been presented by the authors in [69], [64] and unbalanced high-efficiency multi-anode frequency triplers on high-thermal conductivity substrates at 200 GHz and 400 GHz have been presented by Virginia Diodes Inc. in [70]. However, there is a practical limit to the number of anodes based on the chip size, the device impedance, and coupling efficiency. As the number of anodes is increased, compromises must be made between an optimum and even input coupling to the anodes, an optimum matching of each anode at the idler frequencies (second harmonic of the pump frequency for a tripler) and optimum matching at the output frequency.

4.1. In-phase power combining at 300GHz

A complementary approach to increase the power handling of a given source is to power-combine two or more parallel stages. However, for efficient power combining this approach requires increasing care at short wavelengths to keep the parallel paths well-matched despite fabrication and assembly tolerances and to minimize losses in the additional circuits required for dividing and recombining the signal.

We have recently presented results of a 300 GHz frequency tripler that uses two mirror-image circuits power-combined in-phase with a total of twelve Schottky anodes to produce 26 mW at 318 GHz when pumped with 250 mW input power at 106 GHz [71]. This multiplier is based on two mirror-image tripler chips that are power-combined in-phase in a single waveguide block using a compact Y-junction divider at the input waveguide and a Y-junction combiner at the output waveguide. The complete power-combined tripler was designed using the methodology presented previously.

Fig. 4.1 shows the power-combined tripler including the input matching circuit. Fig. 4.2 shows a photograph (rotated 90° clockwise relative to Fig. 4.1) of the waveguide area where the chips are mounted including the output waveguide combiner. The tripler uses a split-block waveguide design with two independent DC bias lines. Each sub-circuit is similar to the 1.7-1.9 THz balanced tripler presented in Fig. 1 but with six anodes per chip instead of two. The input waveguide is split by a Y-junction to evenly feed two circuits each featuring six Schottky planar varactor diodes of about 16 fF each. The chips are mounted in two independent channels, running between the input and output waveguides. The two reduced-height output guides are combined by a Y-junction that is seen by each branch of the circuit as a simple waveguide step. Fig. 4.3 shows the input power, output power and conversion efficiency versus frequency of two power-

combined 300 GHz triplers, while Fig. 4.4 shows the conversion efficiency versus input power of the power-combined 300 GHz tripler and of a single-chip 300 GHz tripler at about 300 GHz.

This was the first demonstration at sub-millimeter wavelengths of this scheme of power combining to enable a 3 dB increase in power handling. In addition to a record of 26 mW obtained at 318 GHz, this frequency multiplier exhibits a record bandwidth.

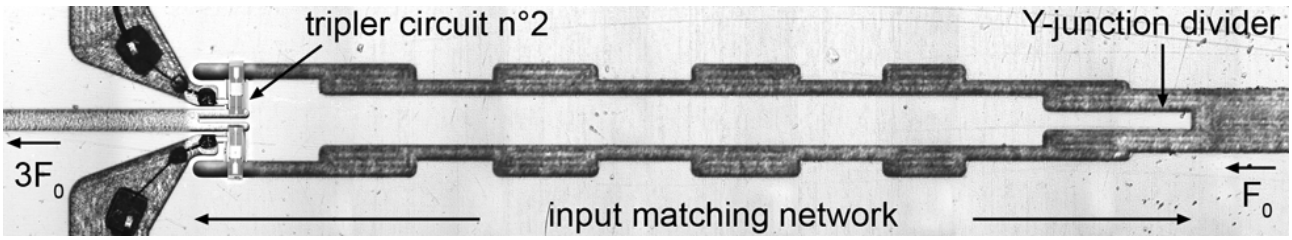


Fig. 4.1. Horizontal view of the bottom half of the power-combined 260-340 GHz frequency tripler based on two mirror-image integrated circuits (design by the author). The dual channel input matching network occupies most of the size of the image.

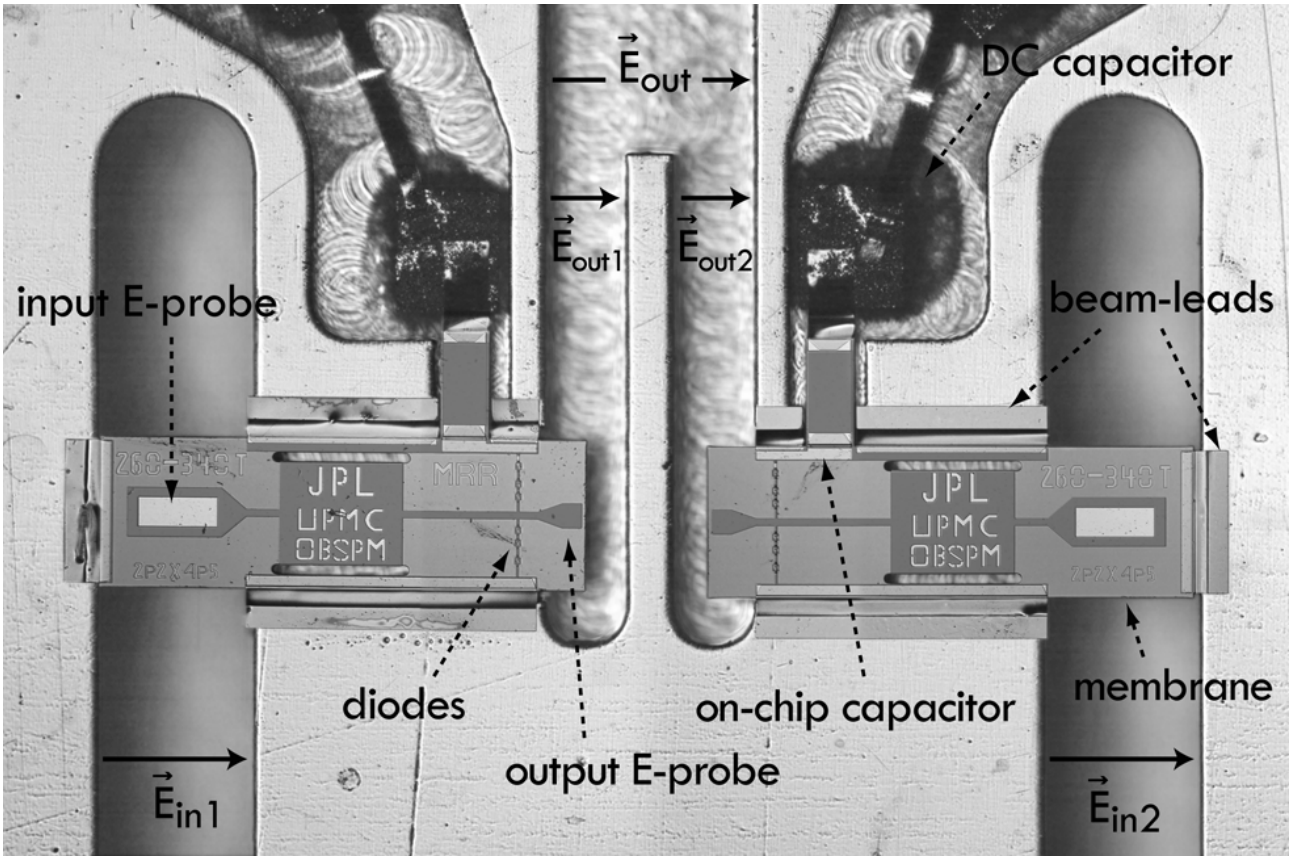


Fig. 4.2 Close-up vertical view of the power-combined 260-340 GHz frequency tripler showing the two mirror-image GaAs integrated circuits. The E-field vectors in the input and output waveguides are indicated by plain arrows. The E-fields generated by the two sub-circuits are combined in-phase in the output waveguide.

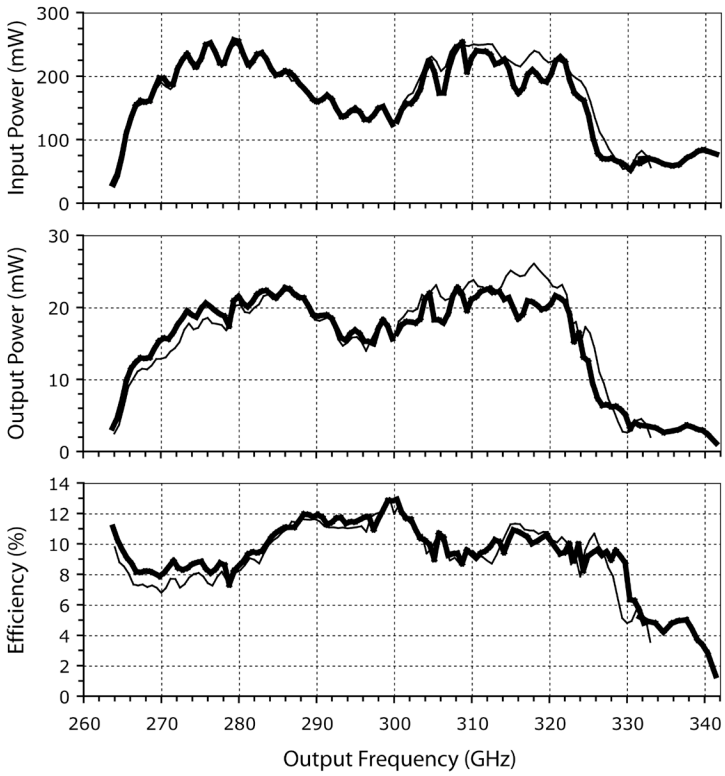


Fig. 4.3. Input power (top), output power (middle) and corresponding conversion efficiency (bottom) across the 265-340 GHz band of two (SN1 and SN2) power-combined frequency triplers. Note that the conversion efficiency is still quite high at the lowest frequency tested. For each graph, the thick curve refers to the SN1 unit while the light curve refers to the SN2 unit. The bias voltages were optimized at each frequency point. The measurements were made using three different power amplifiers to cover 88-114 GHz due to the large fractional bandwidth of the frequency triplers.

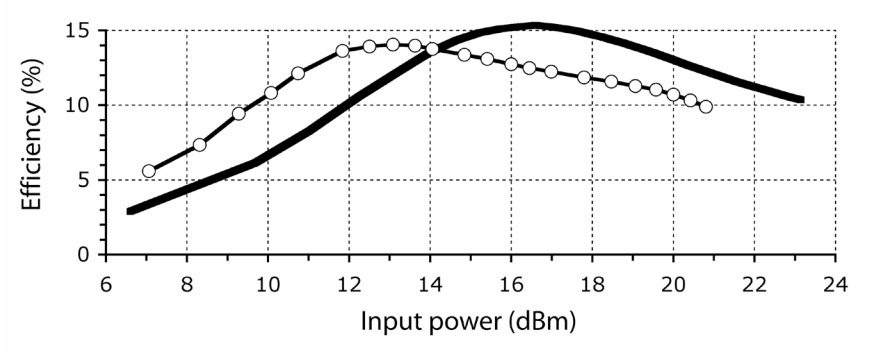


Fig. 4.4. Power sweep of the single-chip tripler at 292.2 GHz (light curve with open markers) and of the power-combined tripler SN1 at 286.2 GHz (heavy curve with no markers). It can be seen that the power-combined tripler begins to compress at an input power which is 3 dB above that of the single-circuit tripler, as expected.

4.2. In-phase power combining at 900GHz

Based on the previous in-phase power combing scheme at 300 GHz, an in-phase power-combined frequency tripler working at 900 GHz was designed to be used as a second stage driver of a 2.7 THz frequency multiplier. Due to the difference of frequency, anode size and input power, the diodes require a different matching circuit than a simple scaled model of the 300 GHz dual-chip matching circuit. In addition the bias circuit requires extra space and forces the use of special bended waveguides that add some constraints in the design.

Fig. 4.4 shows an overall photograph of the tripler including the input matching circuit and two different close-ups of the device area. The tripler uses a symmetrical split-block waveguide design with one device mounted in each half block. Each device features four Schottky varactor diodes monolithically integrated on a 3-micrometer thin GaAs membrane in a balanced configuration and biased in series. Each anode has an intrinsic zero bias capacitance of about 4 fF.

The driver chain of the 900 GHz in-phase power-combined frequency tripler is constituted by a W-band synthesizer followed by a high power W-band amplifier, and a quad-chip power-combined 300GHz frequency tripler based on [71]. When pumped with 330-500 mW, this tripler delivers 29-48 mW in the 276-321 GHz band [72] (these state-of-the-art results are not yet published.)

Fig. 4.5 shows a comparison between the measurements and the simulations while tacking into account the actual input power. Fig. 4.6 shows a comparison of the frequency response of the 900 GHz multiplier chain when cooling from an ambient temperature of 295 K to 120 K from 837 GHz to 937 GHz with a frequency step of 4.5 GHz. The power at W-band does not change with the temperature and is limited to 500 mW since only the 900 GHz tripler and its driver stage are cooled. The 900GHz power-combined frequency tripler produces over 1 mW from 840 GHz to 905 GHz at room temperature with a pick power of 1.3 mW at 860 GHz. The conversion efficiency is in the range of 2.1% to 2.5% in the same frequency range.

The improvement in performance when cooling depends strongly on the frequency. In the center of the band, between 835 GHz and 900 GHz, the improvement varies between 20% at 846 GHz and 90% at 900 GHz. At 928 GHz the improvement is about 100%. At an ambient temperature of 120 K, with a power at W-band limited at 500 mW, the output power peaks at 1.9 mW at 886.5 GHz and at 1.8 mW at 900 GHz. These results (submitted for publication) constitute the state-of-the-art in this frequency range.

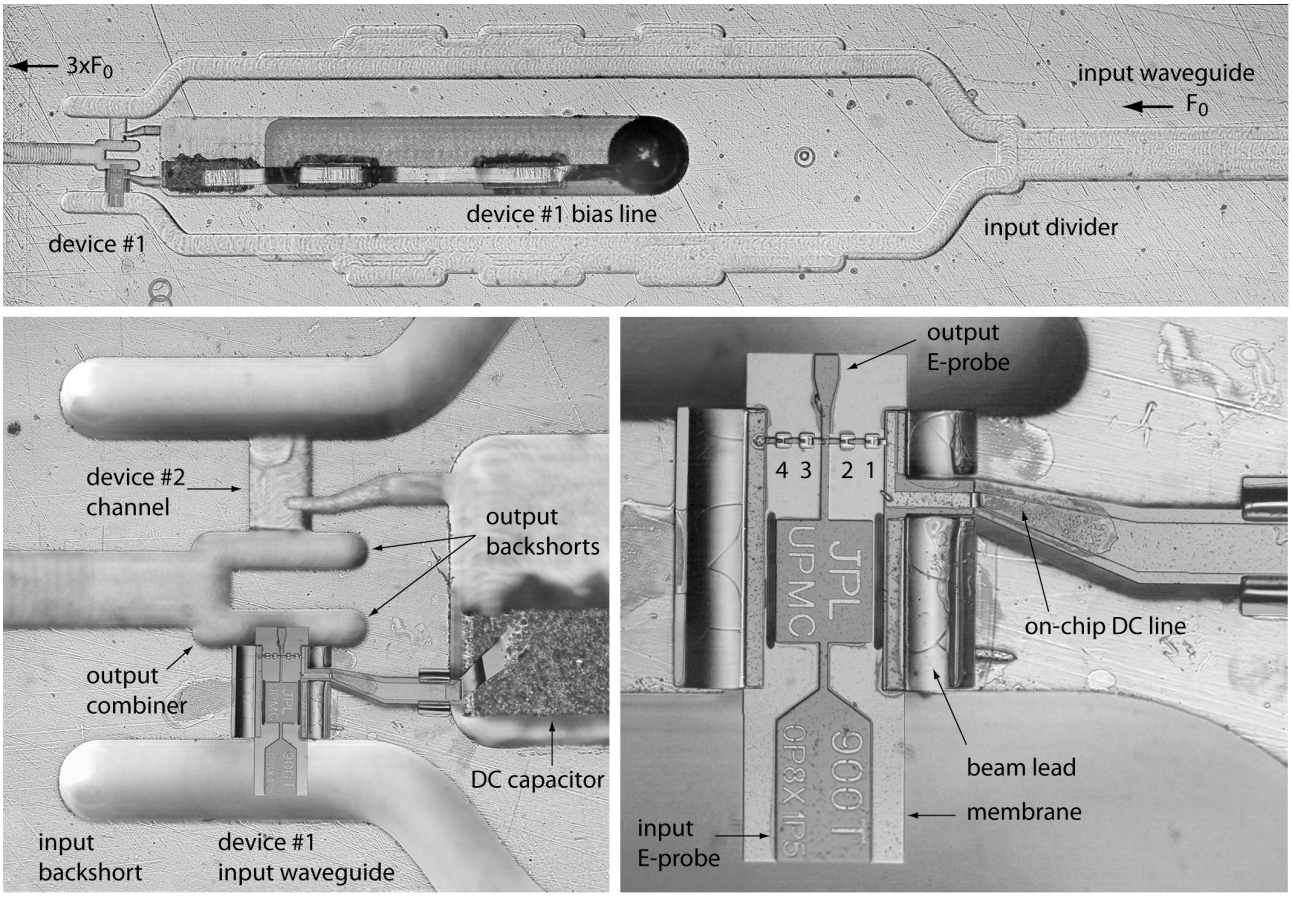


Fig. 4.4 Picture of the bottom half of the power-combined 900 GHz frequency tripler showing device #1 (top view). Close-up view of the output combiner, device #1 and the DC capacitor (bottom left view.) Close-up view of device #1 with labels for diodes #1-4 (bottom right view.). The tripler chip is approximately 300 μm long and 100 μm wide.

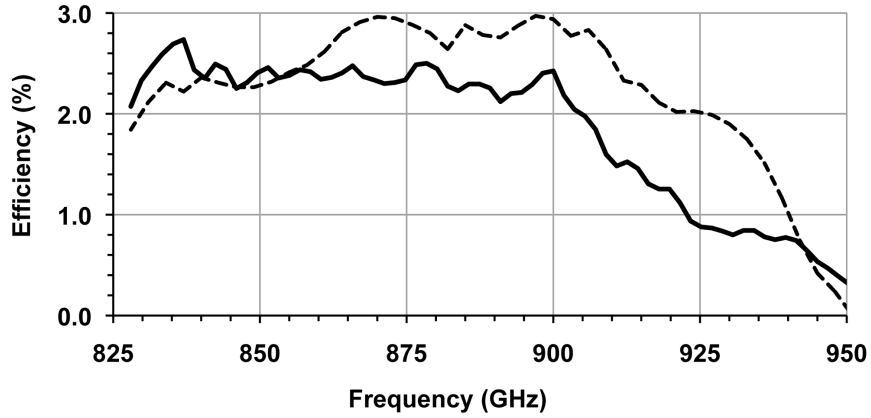


Fig. 4.5. Predicted (dashed-line) and measured (plain line) tripler conversion efficiency of the in-phase power-combined 900 GHz frequency. The measured values of the 900 GHz tripler available input power were used for the simulations.

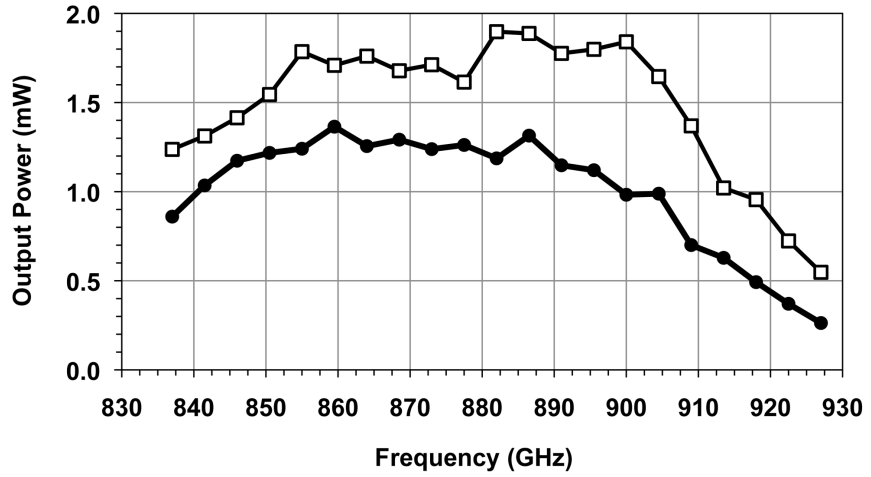


Fig. 4.6. Output power at 120 K (top curve with open markers) and at 295 K (bottom curve with plain markers) of the in-phase power-combined 900 GHz frequency tripler measured with a Thomas Keating power meter and a matched corrugated feed-horn. The measurements were not corrected for the losses of the horn. The bias voltages were optimized at each frequency. The measurements were made using an amplifier that delivers 390-500 mW from 93.0 GHz to 94.5 GHz (837-850.5 GHz multiplier chain output frequency), a fixed 500 mW from 94.5 GHz to 101.5 GHz (850-913.5 GHz multiplier chain output frequency) and 500-395 mW from 101.5 GHz to 103.0 GHz (913.5-927 GHz multiplier chain output frequency).

The spectral purity of the 900 GHz frequency multiplied chain was checked from 0.15 THz to 2.1 THz using a Fourier Transform Spectrometer with 100 MHz resolution. Scans at different frequencies across the band have been performed. The scans where performed at room temperature. Fig. 4.7 shows the measured response at four frequencies covering the center of the band and its edges. The chain spectral purity is remarkably good with spurious or undesired harmonic below -27 dB with respect to the main signal, except at the high end of the band where the second harmonic of the 900 GHz tripler pump signal can be detected at a level of 10 dB below the third harmonic. Although the 100 MHz resolution of the FTS does not allow resolving low frequency spurious around the main carrier nor determine the level of phase noise, extensive tests of such multiplier chains have been done in the past and have shown that spurious and phase noise do not relate to the frequency multipliers themselves but rather to the quality of the power supplies, to the fact that the power amplifiers are saturated or not, and to the phase noise of the synthesizer itself. Fig. 4.7 shows that a cascade of two balance triplers designed to suppress unwanted harmonics can actually achieve that goal at about 1THz.

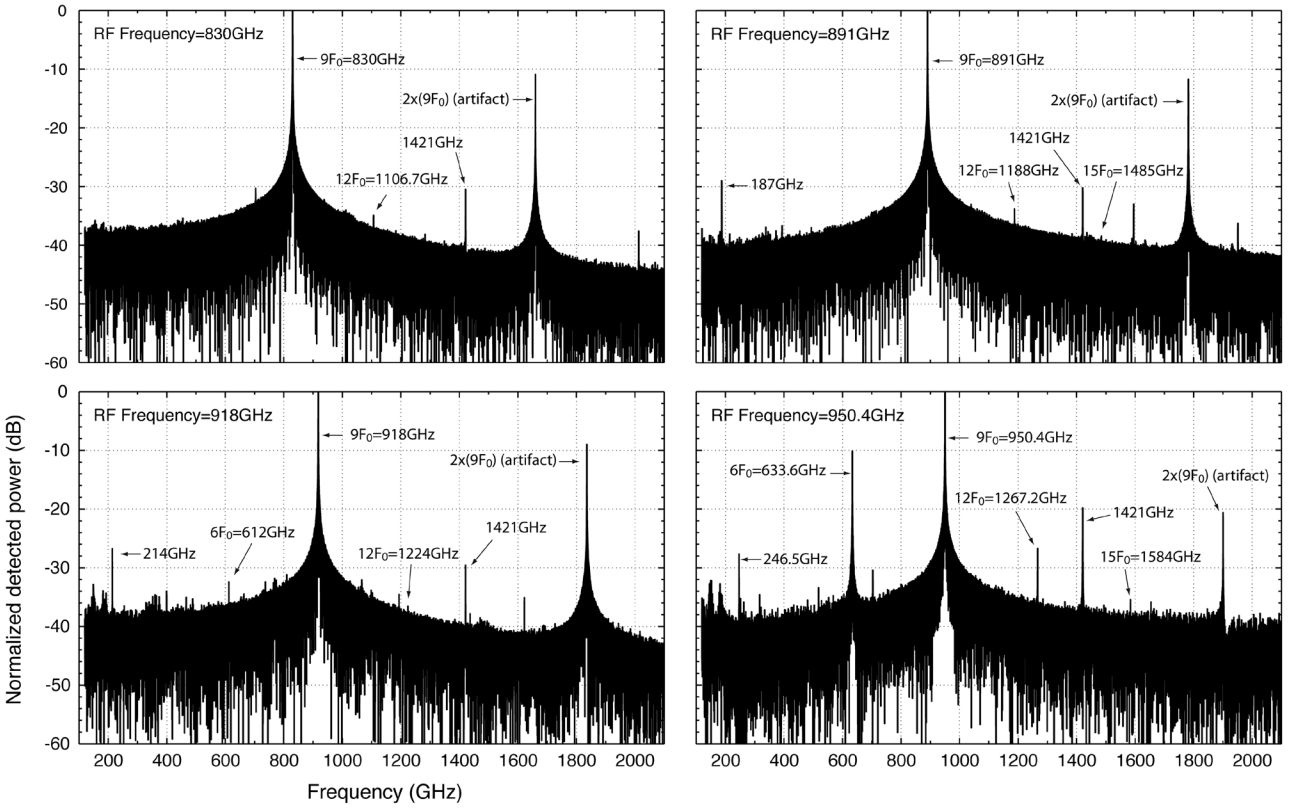


Fig. 4.7. FTS scans with 100 MHz resolution of the 900 GHz frequency multiplier chain at 830.0 GHz (top-left), 891.0 GHz (top-right), 918.0 GHz (bottom-left) and 950.4 GHz (bottom-right). For each scan the graph is normalized to the peak power that corresponds to the 9th harmonic of the input frequency F0 at W-band. Note that the FTS graphs show a strong signal at exactly twice the frequency of the main signal: it is actually an artifact (aliasing) due to the FTS itself.

4.3. Other power combining techniques

The power combining scheme described in section 4.1 and 4.2 has a combining efficiency close to 100% and allows for a two step design-flow that consists in optimizing first the chip and then the waveguide-matching circuit for two chips. An obvious intermediate step is the design of a single chip version of the multipliers before designing the dual-chip version. This approach has the great advantage of decreasing the complexity of the optimization and can make the difference between a converging non-linear simulation and a non-converging one. Nevertheless, this combining scheme can be considered to be at the "circuit level" not at the "chip level". A classic complementary approach consists in using hybrid couplers to combine frequency multipliers. This has the advantage of being well understood and of bringing some isolation between the power combined multipliers, at the expense of an increase of fabrication complexity and RF losses. As a matter of fact this scheme was adopted to design the quad-chip power-combined 300 GHz tripler employed as a driver stage of the 900 GHz frequency tripler presented in section 4.2.

Power combining at the "chip level" is already in place with multi-anode design. One complementary solution that was never exploited in this frequency range consists in designing double-sided circuits, perfectly symmetrical. Technologically it is a very challenging proposition, though not impossible : right-handed and left-handed chips can be assembled using a very-thin layer of a non-conductive low-RF-loss glue. A similar proposition is to leave a well-controlled air-gap in between the two circuits, removing the need of a complex assembly procedure and allowing each chip being mounted in one half of the waveguide blocks, independently of the other. This power combining scheme can be applied to different types of frequency multipliers and is perfectly complementary to the other combining schemes.

In terms of design complexity, it is much more challenging than the others however, in part due to the addition of new propagating modes and to the doubling of the number of devices in the non-linear simulations at the first stage of the circuit optimization. This idea was indeed recently investigated at the Université Pierre et Marie Curie - Observatoire de Paris with a dual-chip multiple-anode dual-symmetry

190 GHz frequency doubler using the Schottky process of the Franco-German commercial foundry United Monolithic Semiconductors [73] (see Fig. 4.8).

Advanced power combining techniques taking the full advantage of the 3 dimensions of the circuits is believed to be one of the keys of pushing solid-state sources working around 300 GHz towards watt-levels and ultimately of pushing sources working well above 1 THz towards milliwatt levels.

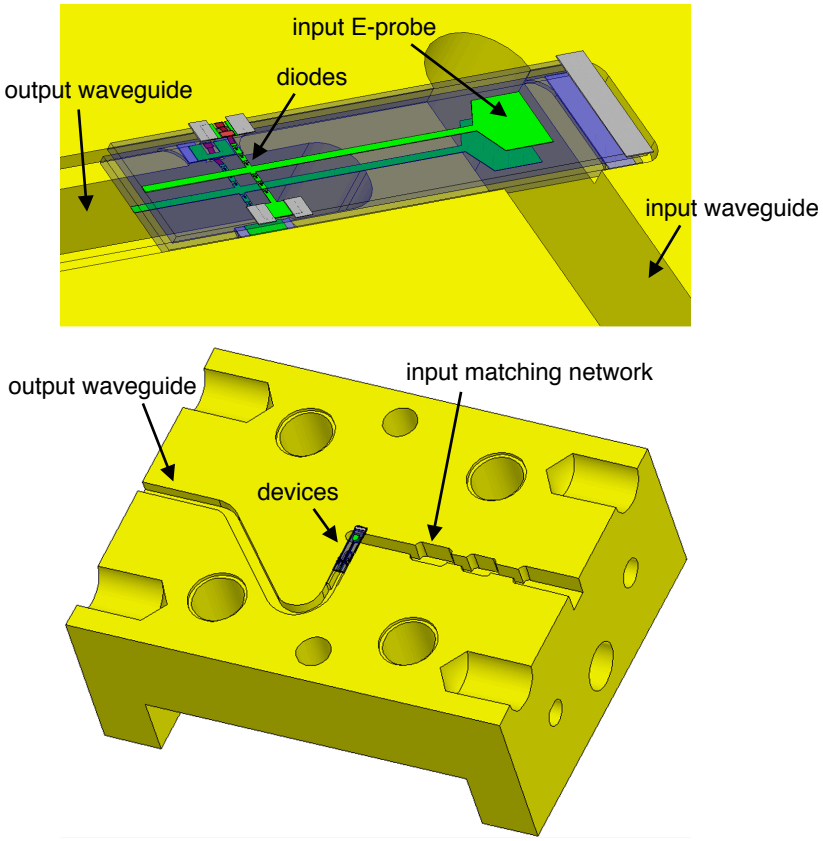


Fig. 4.8. Dual symmetry 190 GHz frequency doubler using UMS Schottky diodes (design José Vicente Siles, at Université Pierre et Marie Curie - Observatoire de Paris). The top view shows a 3D view of the two chips located in the waveguide structure of the multiplier (only the bottom block is shown). The bottom view shows the bottom part of the block with the input matching network (right) and the output waveguide (left.)

4.4. About novel materials and devices

Although GaAs Schottky diodes are still the best device to built high-efficiency sub-millimeter frequency multipliers, they have limited power handling capabilities, mainly due to limited breakdown voltages. On the contrary, GaN Schottky diodes could have very high breakdown voltages and high power handling capabilities. Despite a lower mobility of the carriers in GaN with respect to GaAs, GaN-based Schottky diodes are expected to be well suited to built frequency triplers at 300 GHz [25], [26] provided that the technological steps and the material growth in particular do not degrade this potential.

As mentioned earlier, Heterostructure Barrier Varactor are efficient devices for producing odd-order frequency multipliers : due to the internal symmetry of the device, a HBV-based frequency tripler does not require an idler matching network nor a bias circuit, greatly simplifying the circuit layout. In addition, high breakdown voltage devices can be fabricated by staking several elementary devices in the same epy-layer [60]. This is clearly an advantage for high power HBV-based frequency multipliers that can now produce up to 200 mW at 110 GHz when pumped with 1 W [74].

But HBV frequency multipliers have several limitations: though the lack of bias circuit can be regarded as an advantage other Schottky-based counterparts, it makes HBV devices less flexible to use and harder to match over a broad frequency range. The bias voltage is indeed used to adjust the average capacitance (i.e. impedance) of the Schottky diode depending on the actual pump power and operating frequency. The

average capacitance of a given HBV diode can only be set by adjusting the pump power level. In addition, the active area of HBV diodes is defined by etching the epy-layer contrary to the active area of Schottky diodes, which is defined by a metallic contact on the semi-conductor. The active area of HBV diodes is therefore difficult to reduce to sub-micron dimensions while Schottky diodes as small as 0.2×0.2 μm^2 have successfully been made; this is one of the reasons why no high-efficiency HBV-based frequency multipliers working above 0.5 THz has been demonstrated.

5. Conclusions and perspectives

GaAs Schottky diode technology has advanced dramatically in the last few years to enable power generation via frequency multiplication well into the terahertz frequency range. This development has enabled single pixel space borne terahertz receivers for radio astronomy. To further increase power levels above 1 THz, the priority is currently set on improving the power handling capabilities of the driver stages at millimeter wavelengths, firstly by using advanced power combining schemes, secondly by improving the thermal management at the chip level and finally by exploring new materials.

In the mean time a series of post Herschel THz balanced frequency triplers have been designed at Université Pierre et Marie Curie - Observatoire de Paris and fabricated at the Jet Propulsion Laboratory. They cover the 1.2 THz to 3 THz range. They use a new layout featuring mesas with reduced area, longer air-bridges and a 3 μm-thin membrane that has been removed around the diodes to improve the balance while decreasing dispersions and RF losses (see Fig. 5.1). Preliminary results in the 1.3 THz to 1.5 THz band set new records with up to 100 μW produced at room temperature. Measurements at 2.7 THz have started in early December 2009 and demonstrate the most powerful room-temperature frequency tunable source. This new generation of devices is intended to be used in the future in multi-pixel space-borne or air-borne heterodyne instruments dedicated to astrophysics.

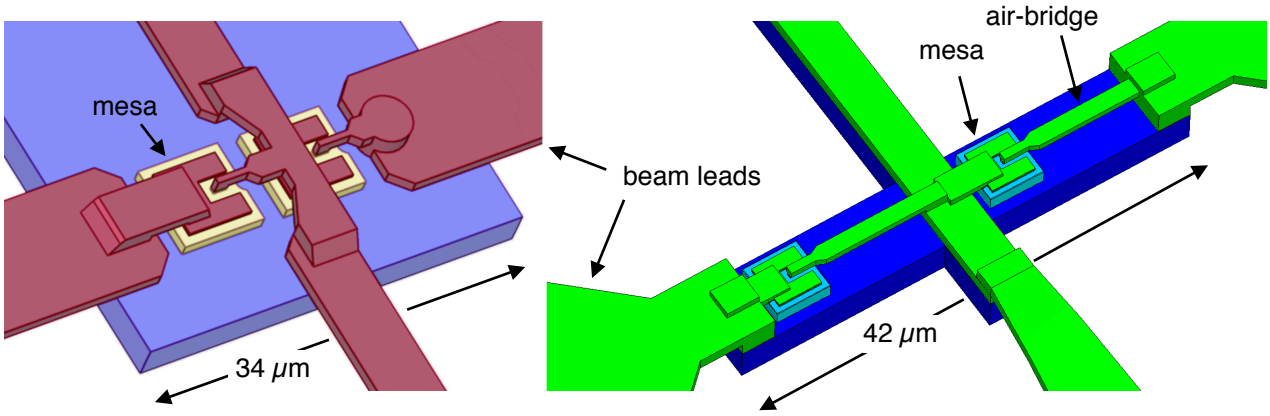


Fig. 5.1. Detail of the diode area of the Herschel 1.9 THz frequency tripler (left) and the post-Herschel re-design version (right). In the later, the mesas have been reduced by 40%, the beam leads land now much closer to the membrane edges allowing longer air-bridges to be implemented in the circuit. The thickness of the GaAs membrane has been kept to 3 μm but the dielectric has been removed around the diodes.

6. References

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