In-Phase Power Combining of Submillimeter-Wave Multipliers

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***Abstract*— Submillimeter-wave multiplier circuits can either be optimized for maximum efficiency or maximum output power depending on the application. However, it is always desirable to have maximum output power without sacrificing efficiency. To accomplish this goal we have proposed and demonstrated in-phase power combining of submillimeter-wave multiplier chips. We report on the design, fabrication and characterization of a 260-340 GHz tripler that utilizes two mirror-image chips and produces a peak of 22 mW with 11% efficiency. This source is then used to drive a two-chip 790-950 GHz tripler. Preliminary results obtained from this LO chain are 0.7 mW at 890 GHz at room temperature. This technology advancement now makes it possible to extend the frequency coverage of multiplier based sources well into the THz range.**

I. Introduction

Broadband, electronically tunable sources based on Schottky diode frequency multipliers continue to be an ideal solution for a number of applications in the THz range[1]. Increasing the output power of Schottky diode frequency multipliers, while keeping them both broadband and with high conversion efficiency, requires designs and technology that can handle higher input power. The use of high thermal conductivity substrates to decrease the anode temperature is a workable solution [2], though this approach can have limitations when working at higher frequencies. Another approach is to design each chip with multiple anodes which we have demonstrated well into the THz region; however, for each design there is a physical limit to how many anodes can be placed on a single chip. To circumvent these limitations we have proposed and demonstrated a simple power combining technology based on well understood components such as Y-junctions. Multiplier chips are combined in-phase to provide a 3-dB increase in output power without sacrificing efficiency and bandwidth. This paper will briefly present the designs and results of in-phase power-combined frequency triplers working in the 260-340 GHz and 790-950 GHz bands.

II. Dual-chip 300 GHz tripler

The power-combined version is based on two mirror-image tripler chips that are power-combined in-phase in a single waveguide block [3]. Each chip features six anodes on a 5 μm thick GaAs membrane. The dual-chip input-matching network features a succession of waveguide sections of high and low impedance and includes a compact Y-junction divider. At the output, a Y-junction combiner is used to combine the power produced by each chip and to match the Schottky diodes at the output frequency.

Figure 1 shows a partial view of the bottom block of the tripler circuit. The input Y-junction along with the two chips is shown in detail. Initial measurements from this circuit have been presented in [3]. Figure 2 shows some complementary measurements made with different input power levels. With an input power of 150 mW, output powers of 18.5 mW at 288.6 GHz and 16.7 mW at 319.8 GHz where measured at room temperature corresponding to conversion efficiencies of 12.3% and 11.1% respectively. Finally, to investigate even higher input power levels, the circuit was pumped with maximum available power (around 250 mW at certain frequency points) and measured output power is shown as the top plot in Figure 2. A maximum output power of 22.5 mW was recorded at 308.4 GHz.

III. Dual-chip 900 GHz tripler

The power combined 900 GHz tripler utilizes two identical 4-anode balanced tripler chips, monolithically fabricated on a 3 μm thick membrane. Contrary to the 300 GHz dual-chip tripler, the two halves of the waveguide block are perfectively symmetrical and have one GaAs chip mounted in each of them (see Figure 3). The tripler is designed to cover the 790-950 GHz band and to be pumped with 30mW. The same method was used for the design as in [3]. Due to the small dimensions of the GaAs chips, implementing the bias line required the use of several waveguide bends to increase the separation between the two paths of the input-matching network. The dual-chip 900 GHz tripler was pumped with the dual-chip 300 GHz tripler (described above) that delivered 12.5-22.5 mW in the 267-315 GHz band at room temperature. The output power of the 900 GHz tripler was measured using an Erickson PM2 power meter and a waveguide transition from WR1.7 to WR10. Preliminary measurements indicate a peak output power of 0.7 mW with a 3-dB bandwidth of 820 to 910 GHz with no corrections for transition loss.

IV. Conclusion

Utilizing this simple power combining approach can lead to higher output power without sacrificing efficiency and bandwidth. Schemes that utilize even more chips in a single block are also being built. Increased output power in the drive stages allows one to then pump later stages with sufficient power. Using this approach can result in multiplier based sources working up to 3 THz with sufficient power to pump single pixel heterodyne receivers.

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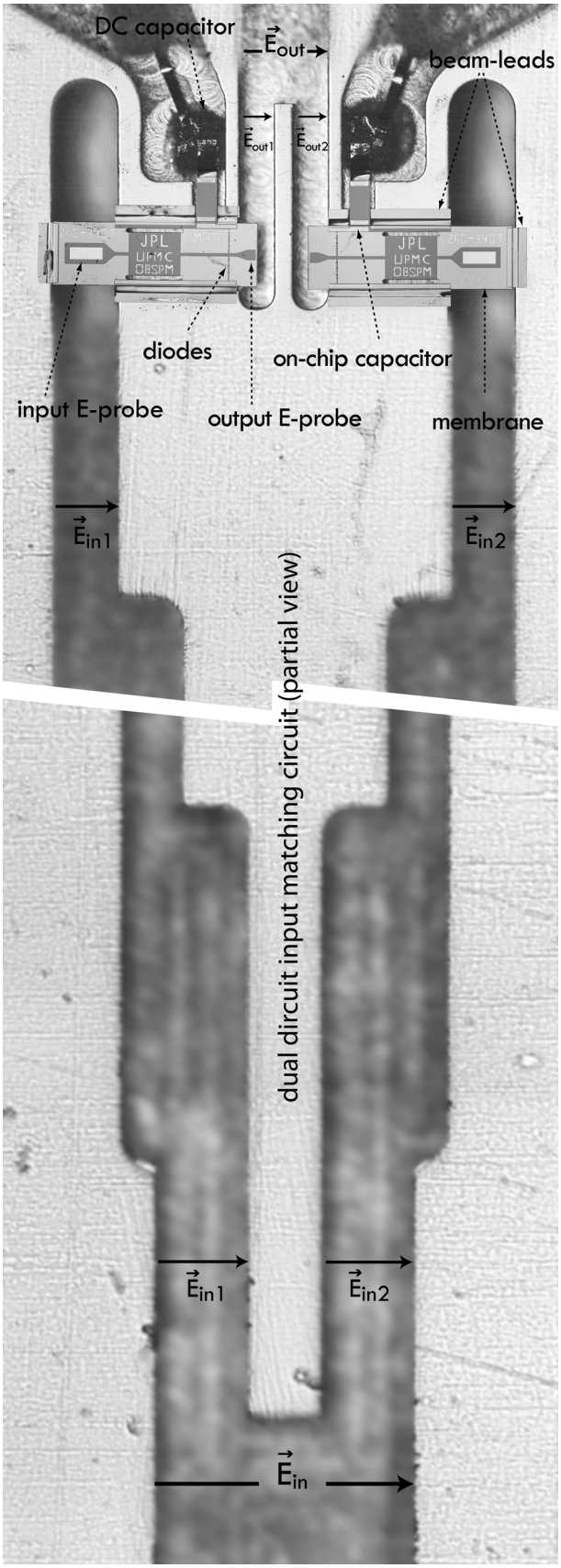

Fig. 1. Partial view of the power-combined 260-340 GHz frequency tripler showing the two mirror-image GaAs integrated circuits. The E-field vectors in the input and output waveguides are indicated by plain arrows.

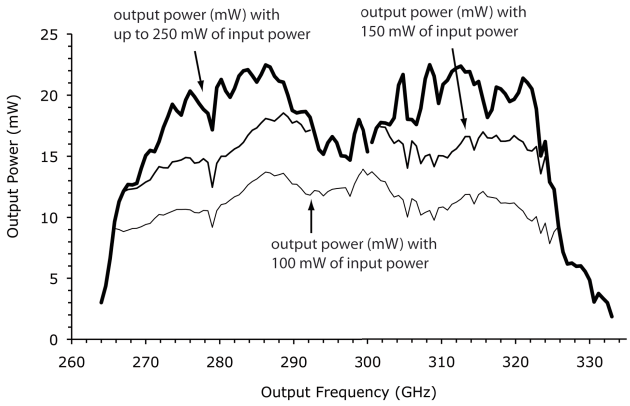

Fig. 2. Output power versus frequency of the 260-340 GHz dual-chip frequency tripler for various input power levels. The top curve is obtained with an input power ranging from 25 to 250 mW. The middle and bottom curves correspond to output powers for respectively 150 mW and 100 mW of input power. Note that the tripler could not be tested with sufficient power below 265 GHz and above 325 GHz.

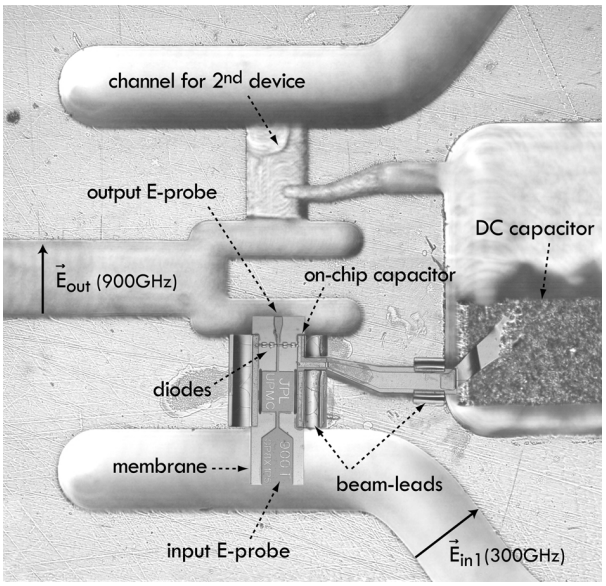

Fig. 3. Close-up view of the bottom block of the power-combined 790-930 GHz frequency tripler with one GaAs integrated circuit. The top block is the exact symmetrical of the bottom block.

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