Monte Carlo Study of 2-D Capacitance Fringing Effects in GaAs Planar Schottky Diodes

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***Abstract*— Nanometer scale planar Schottky barrier diodes (SBDs) with realistic geometries have been studied by means of a 2-D ensemble Monte Carlo simulator. The topology of the devices studied in this paper is based in real planar GaAs SBDs used in terahertz applications, such as passive frequency mixing and multiplication, in which accurate models for the diode capacitance are required. The intrinsic capacitance of such small devices, which due to edge effects strongly deviates from the ideal value, has been calculated. In good agreement with the classical models, we have found that the edge capacitance is independent of the properties of the semiconductor beneath the contact and, as novel result, that the presence of surface charges at the semiconductor dielectric interface can reduce it almost 15%. We have finally provided a compact model for the total capacitance of diodes with arbitrary shape that could be easily implemented in design automation software such as Advance Design System (ADS).**

***Index Terms*— Capacitance–voltage (C–V), edge effect (EE), GaAs planar Schottky diodes, Jupiter ICe moons Explorer Submillimeter Wavelength Instrument, Monte Carlo (MC) simulation.**

I. Introduction

VAST advancements have been done in the development of planar Schottky barrier diodes (PSBDs) for terahertz (THz) local oscillators and heterodyne receivers, since this technology was introduced in the 1990s, thus finally replacing the whisker-contacted Schottky diodes previously used for ultrahigh-frequency applications [1]. Although several technologies are available for building THz sources and detectors, such as quantum cascade lasers, heterostructure barrier varactors, or hot electron bolometers, presently the Schottky technology is the most widespread used, including applications as frequency multipliers from several tens of gigahertz to few terahertz. The good performance of the PSBD-based circuits at room temperature have allowed to implement this technology in ground base and space-borne radio astronomy applications, such as the Herschel Space Observatory [1], [2] and the ALMA observatory [3], [4]. Recently, we are carrying an intense research related to the Submillimeter Wavelength Instrument proposed by the Spatial European Agency in the frame of the future Jupiter ICe moons Explorer mission, working in two frequency channels: 540–640 GHz [5] and 1080–1280 GHz [6]. For the development of such ultrahigh frequency multipliers, it is necessary to have a precise description of the experimental values of the capacitance and resistance of the ultrascaled GaAs PSBDs that are the core of the circuits. Indeed, excellent output power levels have been obtained during the last years by using fitted equations for the experimental capacitance–voltage (C–V) and I–V characteristics of the PSBDs [7], [8]. But such data are not often available, so that the analytical models for the electrical characteristics of SBDs are typically used. The problem is that when reducing the size of the diodes for increasing the frequency of operation, the emergence of nonideal phenomena can affect the accuracy of the models used in the circuit design process and thus dramatically reduce the final efficiency of the multiplication stage [4], [9], [10]. The advanced physical models used at JPL (including not only fringing capacitances in the equivalent circuit of the PSBDs, but also carrier inertia, influence on the resistance of the doping-dependent mobility, and so on, as explained in [6] and [11]) have allowed to reach the output frequencies of 1.5 THz [4]. But just the use of the simple model for the edge capacitances proposed in [9], jointly with an adequate modification of the value of the series resistance of the diodes (which has to be artificially increased), has allowed the increase of the output frequency of frequency multipliers up to 2.48–2.75 THz [12]. However, none of these models can accurately predict the output power of the circuits, and good agreement between simulations and measurements can only be obtained if the models are adjusted once the experimental results are available. Therefore, the key point for the correct operation of the fabricated circuits is the experience of the designer in adequately tuning the values of the electrical parameters used in the models of the PSBDs. Since the most important parameter for optimizing the performance of frequency multipliers is the nonlinearity

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of the C–V characteristic of the diodes, we will reassess the validity of the capacitance models used in the design of such applications, which are critical mainly when aiming at high-efficiency or high-power circuits at the frequencies of the pump signal above 100 GHz. Also the I–V curve of the devices has to be correctly modeled, but this point is out of the scope of this paper.

We have to stress that the lumped-element circuit (LEC) model is valid in a certain frequency range, since, even if using correct values for the capacitances and resistances of the PSBDs, such model fails when increasing the input frequency. For this sake, we refer to the results shown in [13], where a review of the available models for the design and optimization of Schottky diode-based multipliers is made. Pardo *et al.* [13], using an harmonic balance circuit solver coupled to an LEC representation of the diode (LEC-HB), compared the results provided by drift-diffusion and hydrodynamic transport models with those obtained with a 1-D Monte Carlo (MC) simulator (also coupled with the HB solver, MC-HB). The MC simulator is considered as a reference when comparing the different models of Schottky diodes, since, by accounting for all the microscopic phenomena taking place within the devices, it provides a precise description of the semiclassical electron transport even under large signal or high frequency excitations. The main conclusion extracted in [13] is that the operation of Schottky-diode-based circuits up to very high frequencies (even above 1 THz) can be correctly described by means of simplified analytical LEC-HB simulators as long as correct values for the resistances and capacitances are used, which can be provided by means of MC simulations.

However, this conclusion is only valid as long as velocity saturation and carrier inertia phenomena are absent, i.e., at frequencies below a certain limit. Fortunately, the effect of velocity saturation can be avoided in experimental applications by reducing the bias and increasing the epilayer doping [14], thus allowing the LEC models to be valid for well-designed diodes at input frequencies even above 600 GHz (i.e., triplers approaching output frequencies of 2 THz). This result has been confirmed by dynamic simulations of the GaAs PSBDs studied in this paper, carried out with our 2-D MC code, in which the influence of velocity saturation phenomena is not significant at input frequencies below 300 GHz. Above this limit, physical models accounting for these phenomena are necessary, as discussed in [11].

In this context, the aim of this paper is to calculate, by means of MC simulations, the static capacitance of GaAs PSBDs to be used in the design of THz circuits using LEC-HB models, and also analyze the microscopic origin of the fringing capacitance. To this end, we will use the 2-D MC simulator presented in [15] and [16]. From the calculated values of the capacitance, we propose a simple compact analytical model for the C–V dependence, accounting for the influence of the surface charges on edge effects (EEs), which correctly describes the obtained results and can be readily included in commercial nonlinear HB simulators. This analysis is especially important for high-frequency applications, where the anode surface needs to be drastically reduced as the frequency increases and the available power is low, so that a precise design for an improved efficiency is highly demanded. The so-called "EE" becomes important for such small PSBDs and can strongly modify the optimal conversion efficiency point. Previous studies of the EE have been performed by different authors [17], [18], but always considering an ideal epilayer–dielectric interface in the proximities of the Schottky contact, i.e., disregarding the depletion region present at the semiconductor surface originated by trapped charges. The aim of this paper is to shed light on the microscopic origin of the EE in the capacitance of PSBDs, including the contribution of surface charges. The influence of the epilayer structure and the surface charges at the semiconductor–dielectric interface on the EE capacitance will be quantified in order to provide a compact model that can be easily implemented in design automation software such as ADS, which will allow the precise design of THz monolithic microwave integrated circuits based on GaAs PSBDs.

This paper has been structured as follows. In Section II, the physical simulator based on the 2-D MC method and the geometry of the PSBDs are introduced. In Section III, the analytical model to characterize the charge variations in Schottky diodes derived from the MC results is presented, as well as the influence of the surface potential on the depletion region generated by the Schottky contact. A geometrical analysis is also carried out in this section to identify the physical origin of the observed charge variations and associated capacitance. Our main conclusions are finally drawn in Section IV.

II. Physical Model

A. Monte Carlo Simulator

This paper has been performed by using a semiclassical ensemble MC simulator of carrier transport self-consistently coupled with a 2-D Poisson solver. Three nonparabolic spherical valleys (Γ, L, and X) are used to model the conduction band of the GaAs semiconductor layers [19]. Ionized impurity, alloy, polar and nonpolar optical phonon, acoustic phonon, and intervalley scattering mechanisms are taken into account, allowing the consideration of hot carrier effects in the proximities of flat-band in Schottky contacts [20]. Fermi–Dirac statistics, using a self-consistent calculation of the Fermi level, are imposed for the occupancy of energy states by means of the rejection technique when selecting the final state after scattering events [16]. This technique has already been successfully applied for the study of HEMTs [21]–[23]. Regarding the contact models, both the Schottky and the ohmic contacts are simulated as in [16] and [20]–[23]. The Schottky contact is simulated as a perfect absorbing boundary, that is, all the carriers reaching the metal contact leave the structure and no carriers are injected from the metal into the semiconductor. This consideration leads to the modification of the Maxwellian velocity distribution of the electrons at some tens of nanometers from the Schottky interface to a perfect hemi-Maxwellian distribution at the interface [24]–[26]. Regarding the ohmic contact model, it imposes charge neutrality in the proximities of the electrode by injecting carriers with the appropriate thermal distribution (velocity-weighted hemi-Maxwellian) at the lattice temperature [20].

In this paper, we focus on the determination of the junction capacitance as a function of the applied voltage (in reverse and forward bias below flat-band conditions) in 2-D PSBDs. The junction capacitance in Schottky diodes is associated to bias-induced variations of the depletion region generated by the built-in voltage of the junction and the applied voltage. Additional (bias independent) depletion regions originated by the presence of surface charges at the semiconductor–dielectric interfaces can overlap the previous one, thus affecting the value of the junction capacitance. Such surface charges are accounted for in the simulator by means of the model used in [15], in which the value of the considered surface charge, σ, is related to that of a surface potential, V_S, by

$$\sigma = -\sqrt{2qN_D|V_S|\varepsilon_{SC}} \tag{1}$$

where N_D is the semiconductor doping, ε_{SC} is the permittivity of the semiconductor, and q is the electron charge. A frequent criterion to choose the V_S value considers that it is the surface potential necessary to bring the Fermi level of the semiconductor near the middle of the bandgap [16]. We will study the influence of the surface charges by simulating different Fermi-level pinning conditions, with the values of V_S ranging from 0 V to a maximum of −0.7 V, the half of the GaAs bandgap.

To compute the dc capacitance of the PSBDs, we monitor the average number of electrons present inside the diode at every bias point. The intrinsic capacitance is then calculated from the charge variation from point to point as $\Delta Q/\Delta V$, neglecting the dielectric capacitance between contacts, whose value is much smaller, and the parasitic contributions of the accesses.

B. Simulated Structure

The MC simulated structures are based in real PSBDs fabricated using the E-beam photolithography LERMA-LPN process, presented in [27] and [28]. Fig. 1(a) shows an image of a real PSBD used in a frequency doubler at 280 GHz, which is part of the local oscillator (LO) chain of the 600-GHz frequency receiver presented in [5]. The red line indicates the transversal plane where the 2-D MC simulated structure has been defined. Taking advantage of the symmetry of the anode, only half of the diode is considered in the simulation domain for reducing the computational requirements. The scheme of the simulated PSBDs is shown in Fig. 1(b), where the characteristic lengths are indicated. The GaAs layer structure consists of a highly doped n$^+$ substrate (with doping N_S) and an n epilayer (with low doping N_E). The Schottky contact is placed on the top of the epilayer, while the ohmic contact is deposited on the semiconductor substrate and isolated from the epilayer by etching and dielectric deposition (Si_3N_4), which also passivates the global structure. The simulated surface charges σ are placed at the epilayer–dielectric and substrate–dielectric interfaces [in red in Fig. 1(b)] and their value (for a given V_S) is calculated following (1), according to the doping level of each semiconductor layer.

The simulated geometry resembles as closely as possible the fabricated PSBD. The substrate thickness W_{Sub} and the ohmic contact length L_{OhmL} are large enough to ensure a flat

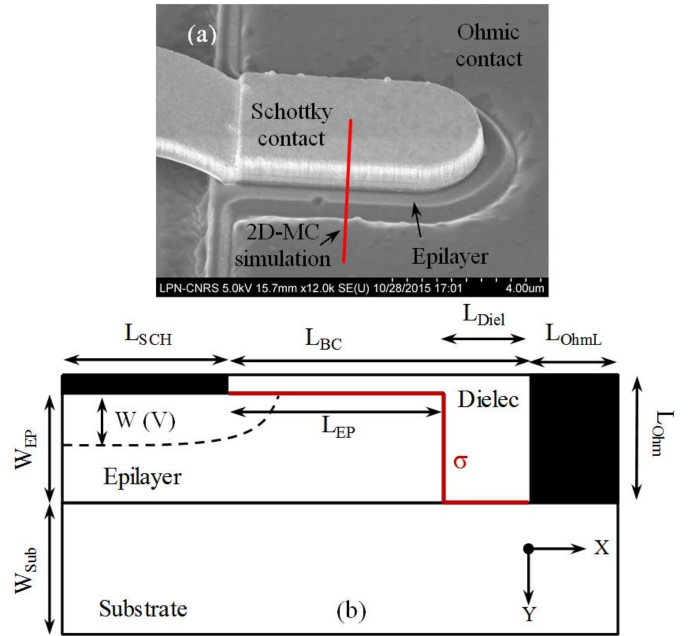

Fig. 1. (a) Image of a real PSBD fabricated by LERMA-LPN-CNRS. (b) Scheme of the MC simulation domain based in the real devices.

TABLE I
PHYSICAL AND GEOMETRICAL PARAMETERS OF THE TWO SIMULATED PSBDs

Symbol	DiodeA	DiodeB
L_{SCH} (nm)	200	1500
W_{EP} (nm)	180	350
L_{EP} (nm)	230	460
L_{Diel} (nm)	120	240
L_{BC} (nm)	350	700
W_{Subs} (nm)	350	500
L_{OhmL} (nm)	300	500
N_E (cm^{-3})	$3\cdot10^{17}$	$1\cdot10^{17}$
N_S (cm^{-3})	$5\cdot10^{18}$	$5\cdot10^{18}$
V_B (V)	0.745	0.695

potential profile at the bottom of the structure. The length of the dielectric region L_{Diel} that isolates the ohmic contact from the epilayer is similar to the epilayer thickness W_{EP}, determined by the technological process [29], [30].

The simulated Schottky anode length L_{SCH}, and the epilayer length between contacts L_{EP}, thickness W_{EP}, and doping level N_E will be modified to study the influence of the epilayer geometry on the depletion region generated by the Schottky contact. Since this paper is focused on the study of the backward junction capacitance of the PSBD, which is especially important in multiplying applications, the epilayer thickness in the simulated structures will be always large enough to avoid the penetration of the depletion region into the substrate layer in the applied bias range [31].

According to these considerations, two different structures, presented in Table I, have been defined to carry out the study. The DiodeA structure is based on a PSBD used in the frequency mixer presented in [5] but with a thicker epilayer to

allow for higher reverse biasing, while the DiodeB structure is based on the frequency doubler of the same receiver. These structures present a very different Schottky anode size L_{SCH} and a different epilayer doping level N_E. The lengths L_{OhmL} and W_{Subs} are sufficiently large to avoid any artificial resistance coming from the simulation of the ohmic contact or the substrate. The geometry of the epilayer (W_{EP}, L_{EP}) is defined according to its doping level to ensure that the depletion region does not reach the substrate layer or the vertical epilayer–dielectric interface placed at a distance L_{EP} from the edge of the anode. Initially, a value of -0.5 V is considered for the surface potential V_S; then, it will be modified in order to analyze its influence on the PSBD capacitance.

III. Results

From the integration of the number of particles inside the diode obtained with the MC simulation for each bias point, we evaluate the variation with the bias of the total charge in the structure (and hence the capacitance), which can be associated to the variation of the depletion region generated by the Schottky contact. The charge variation has been analyzed in the bias steps of 0.5 V when strongly reverse biasing the diode and 0.05 V when near flat-band conditions. The C–V characteristics of nanometer scale GaAs PSBDs with realistic geometries (as shown in Table I) will then be obtained.

The simulations are also able to show the local contribution of the different regions of the device to the charge variation (and to the total capacitance of the diode) by subtracting the electron concentration in each cell of the mesh structure at two different bias points, as shown in Fig. 2. As clearly observed in the figure, the intrinsic capacitance of PSBDs deviates from the ideal value of a parallel-plate capacitor due to the presence of a depletion region not only below the anode but also around its edge. Moreover, the variations of the bias-induced depletion region (and therefore the total junction capacitance) become strongly affected by the presence of surface charges when these are considered in the simulations, Fig. 2(b) and (d), mainly because of a decreased contribution of EEs.

The results of the 2-D MC model for the depleted charge (per unit length in the nonsimulated dimension, thus in C/m) will be compared with the ideal value of the charge in the depletion region generated by the Schottky contact in the absence of EEs [32]

$$Q_{\mathrm{Ideal}}(V) = -L_{\mathrm{SCH}} q N_E W(V) = -L_{\mathrm{SCH}} \sqrt{2q\varepsilon_{\mathrm{sc}} N_E (V_B - V)} \tag{2}$$

where V_B is the built-in voltage of the Schottky contact, V is the applied bias, and

$$W(V) = \sqrt{\frac{2\varepsilon_{\mathrm{sc}}(V_B - V)}{qN_E}} \tag{3}$$

is the depth of the depletion region. In the MC simulation, the charge depleted by the bias voltage Q_{MC} is calculated as the difference between the total charge in the diode for a given bias and that present under flat-band conditions.

The dependence of the depleted charge on the bias (below flat-band) obtained with the 2-D MC simulations of DiodeA

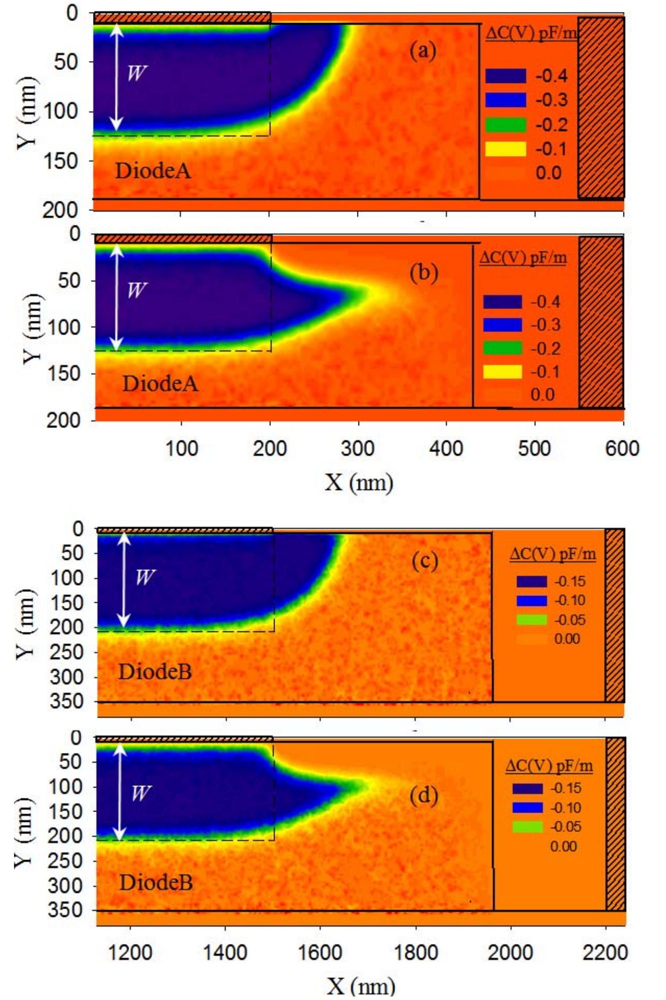

Fig. 2. Map of the local contribution to the total capacitance per unit length (calculated as the variation of the charge per unit length between the bias points $V = V_B$ and $V = -2$ V, divided by the voltage difference) for both (a) and (b) DiodeA and (c) and (d) DiodeB. The MC simulations are performed considering (a) and (c) a null surface potential and (b) and (d) $V_S = -0.5$ V. The depth of the depletion region calculated within the total depletion assumption, W, is shown, and the rectangular shaded region indicates the depletion region expected for an ideal parallel-plate capacitor. Note that the axes have been scaled between DiodeA and DiodeB due to the different size of the diodes.

and DiodeB, normalized to the simulated anode length, is shown in Fig. 3(a) when a surface potential $V_S = -0.5$ V is considered. While in both diodes the expected $(V_B - V)^{1/2}$ dependence of the depleted charge is followed, there is a discrepancy when comparing the MC results with the ideal charge variation given by (2). A larger difference is observed for DiodeA, mainly because it has a smaller size (lower L_{SCH}). However, if the ideal depleted charge given by (2) is subtracted from the MC results, and we remove the normalization by the length L_{SCH}, the resulting difference is practically the same for both diodes, as shown in Fig. 3(b). Fig. 3(b) also shows that the additional depleted charge due to the EE presents a linear dependence on the bias (in reverse bias, far from flat-band conditions), in good agreement with previous predictions [17], [18].

This result indicates that the additional charge contribution originated from the 2-D geometry of the diodes (EE)

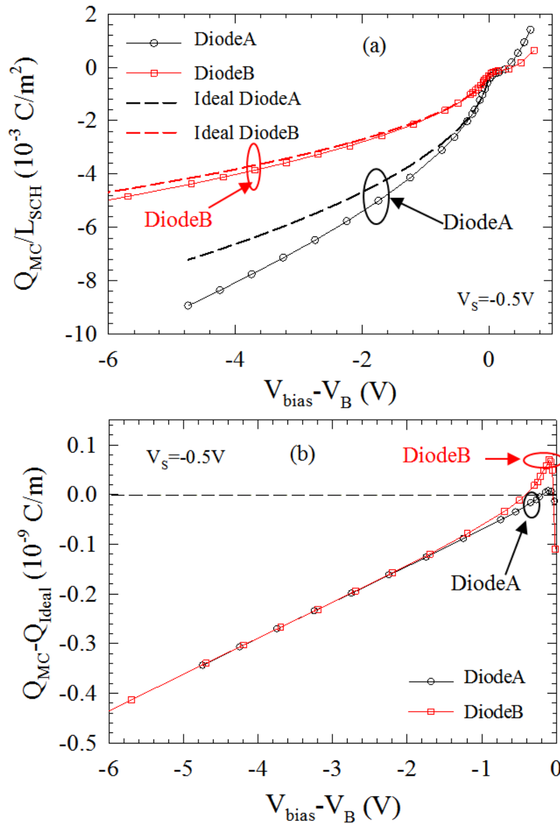

Fig. 3. (a) Depleted charge per unit surface, obtained by normalizing by L_{SCH} the charge per unit length obtained with 2-D MC simulations, compared with the ideal one (dashed lines) for DiodeA and DiodeB. (b) Excess charge per unit length depleted at the edges of the Schottky contact due to 2-D phenomena calculated by subtracting the ideal charge given by (2) from the 2-D MC result. A surface potential $V_S = -0.5$ V has been considered in these simulations.

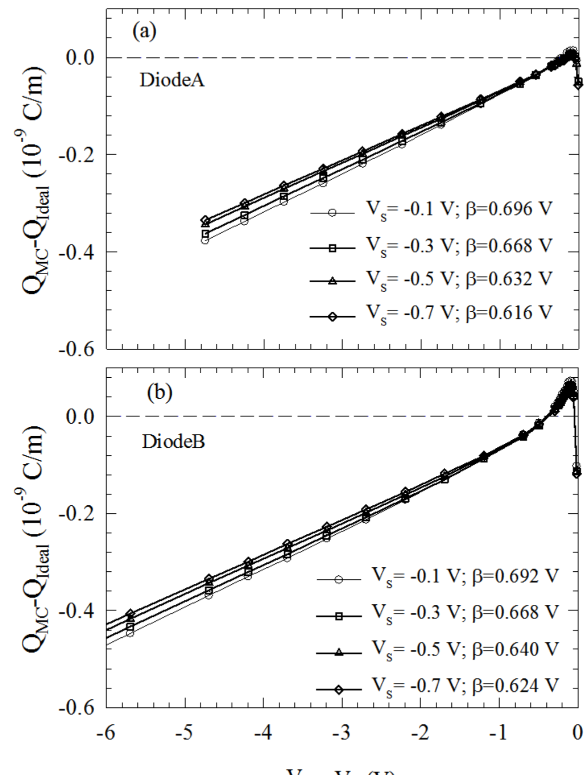

Fig. 4. Charge per unit length depleted by the Schottky contact in excess of the ideal value given by (2) ($Q_{\mathrm{MC}-}Q_{\mathrm{Ideal}}$) for (a) DiodeA and (b) Diode B when considering $V_S = -0.1$, -0.3, -0.5, and -0.7 V.

is independent of the anode size and doping level of the epilayer, result already obtained in analytical calculations of the electric potential distribution in metal–semiconductor junctions [33], [34]. Indeed, we have performed simulations in a large variety of diodes and all of them follow this universal behavior. However, it is important to remark that the description of the response of PSBDs at very high frequencies (above the range of validity of the standard LEC approach) requires more than a single capacitance to account for complex nonharmonic effects related to velocity saturation, which do depend on the doping level of the epilayer [13].

As shown in Fig. 2, this 2-D EE observed with our MC model is strongly dependent on the presence or not of surface charges at the semiconductor–dielectric interface. We can therefore analyze the influence of the surface potential of the epilayer on the additional depleted charges associated to the 2-D effects by plotting, Fig. 4, the difference between the MC results and the ideal depleted charge ($Q_{\mathrm{MC}} - Q_{\mathrm{Ideal}}$) for different values of V_S. As observed, it is possible to conclude that the linear tendency remains for any surface potential considered in the simulation, but with a slope that slightly depends on V_S.

According to the previous observations, and in agreement with the classical models [17], [18], we can propose a modification of (2) able to account for the 2-D effects appearing in PSBDs by including an additional linear term, and considering a dependence of the EE parameter on the surface potential

$$Q(V) = -L_{\mathrm{SCH}}\sqrt{2\varepsilon_{\mathrm{sc}} q N_E (V_B - V)} + \beta(V_S)\varepsilon_{\mathrm{sc}}(V - V_B) \tag{4}$$

where $\beta(V_S)\cdot\varepsilon_{\mathrm{sc}}$ is the slope of the representation of $Q_{\mathrm{MC}} - Q_{\mathrm{Ideal}}$ versus $V - V_{\mathrm{B}}$ [Figs. 3(b) and 4] with $\beta(V_S)$ the dimensionless EE parameter. This parameter was already defined in [17] and [18] as a phenomenological way of characterizing EEs in PSBDs, but it was taken as a universal constant. In fact, (4) highlights that the EEs do not depend neither on the anode size nor on the doping level of the epilayer. However, our MC simulations clearly show that the value of the EE parameter can be affected by the presence surface charges at the epilayer–dielectric interface.

From the fitting of the MC results with (4), we have extracted the dependence of β on V_S and plotted it in Fig. 5 for both simulated diodes. We can observe that, in spite of the differences in the geometry and doping levels, DiodeA and DiodeB show very similar values of the EE parameter. This result is coherent with the classic model first proposed in [17] and extended in [18], in which a parameter called D_1 is proposed for characterizing the EE, with a universal value of 0.36, which coincides with our calculations in the absence of surface charges (since $\beta_0 \equiv 2D_1 = 0.72$). The decrease of $\beta(V_S)$ with increasing negative values of V_S shown in Fig. 5 is connected with the lower charge variations at the edge of the Schottky contact due to the depletion

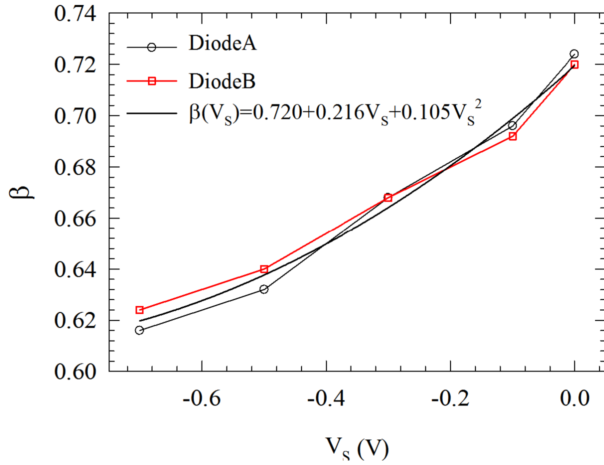

Fig. 5. EE parameter variation when considering a surface potential sweep from 0 V to −0.7 V for DiodeA and DiodeB. An analytical approximation of $\beta(V_S)$ in the considered range is included.

induced by the surface charges at the semiconductor–dielectric interfaces, as clearly shown in Fig. 2(b) and (d).

We can then propose a second-order polynomial approximation for $\beta(V_S)$ that can be considered to be universal according to the MC results, since it is independent of the properties of the semiconductor beneath the contact, and so is the edge capacitance (as we will show next)

$$\beta(V_S) = 0.720 + 0.216 \cdot V_S + 0.105 \cdot V_S^2 \tag{5}$$

where $V_S < 0$ is defined in volts.

Starting from the analytical expression for $Q(V)$, given in (4), we can straightforwardly extend our analysis to the behavior of 2-D EE in the capacitance of PSBDs, and provide a simple analytical expression to obtain the value of the capacitance per unit length of the PSBDs, $C(V)$, as

$$\begin{aligned} C(V) &= \frac{dQ(V)}{dV} = L_{\mathrm{SCH}}\frac{\varepsilon_{\mathrm{sc}}}{W} + \beta(V_S)\varepsilon_{\mathrm{sc}} \\ &= C_{\mathrm{Ideal}}(V) + C_{\mathrm{EE}} \text{ (in F/m)}. \end{aligned} \tag{6}$$

Equation (6) reveals a deviation from the ideal parallel-plate capacitance, $C_{\mathrm{Ideal}}(V)$, due to the presence of a constant contribution to the total capacitance of the PSBD, $C_{\mathrm{EE}} = \beta(V_S)\varepsilon_{\mathrm{sc}}$, originated by the 2-D EEs, and whose value is only dependent on the dielectric constant of the semiconductor and the parameter $\beta(V_S)$.

In Fig. 6, the results of the MC simulations using three different values of V_S are compared with the analytical expression (6) [using the values of $\beta(V_S)$ provided by (5)] and the ideal parallel-plate capacitance $C_{\mathrm{Ideal}}(V)$. Due to the EE, $1/C^2$ is not a straight line anymore, but it is deviates from the ideal behavior. Such deviation is more pronounced in DiodeA as the anode size is reduced, since the ideal contribution decreases while the contribution of C_{EE} remains constant. The implementation of this capacitance model in a nonlinear HB simulator and its usefulness with respect previous models is a matter of a different analysis, but the conclusion obtained in [18] has already been verified: the presence of EEs in small anodes leads to a more reactive impedance of the PSBD as the excited voltage signal enters in the inverse region, what leads

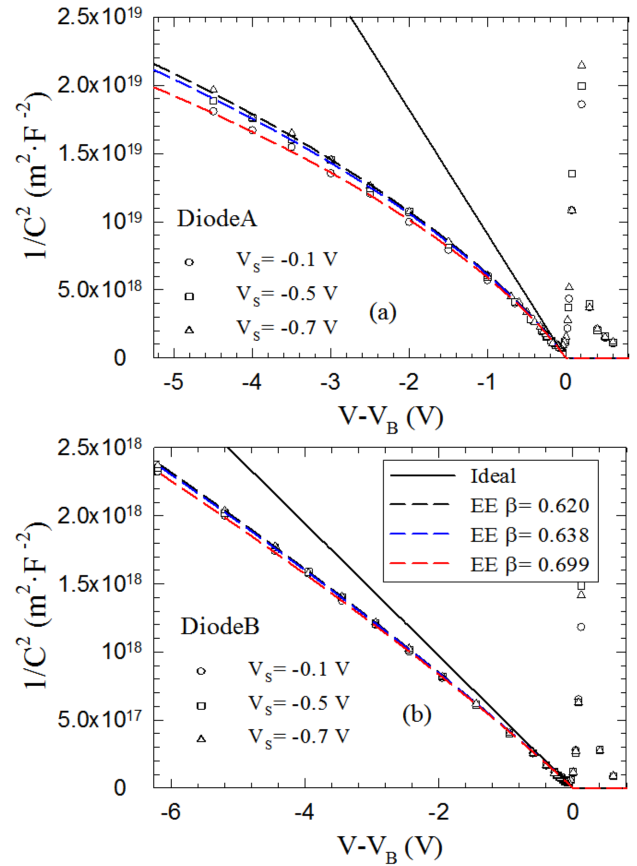

Fig. 6. Comparison between the values of $1/C^2$ in (a) DiodeA and (b) Diode B obtained with the MC simulations (symbols) and the analytical expression of (6) (dashed lines) when considering $V_S = -0.1$, -0.5, and -0.7 V. Black solid line: ideal parallel-plate capacitance of Schottky diodes.

to a reduction of the conversion efficiency of the multiplier as well as to a modification of the optimal bias.

In conclusion, (5) and (6) are able to correctly reproduce the results of the capacitance of PSBDs obtained with the MC simulations, so that they could even be used to extract the values of V_S from the measurements of the C–V curve of any kind of PSBDs. However, this analysis is extremely difficult, since the parasitic contributions to the intrinsic capacitance of the PSBD should first be deembedded. Indeed, for practical design purposes, EE and parasitic contributions could both be included in (6) just by modifying the value of β, so that this simple compact model for the PSBD capacitance can be easily implemented in commercial circuit simulators such as ADS.

We must remark that our study of EEs has been performed with a 2-D representation of a rectangular Schottky anode, assuming the diode is homogenous in the nonsimulated dimension. This means that in a realistic case of a Schottky contact with a given geometry, to calculate the additional contribution of EEs to the absolute diode capacitance, C_{EE} should be multiplied by the total length of the diode contour.

In addition, in the case of circular anodes a further correction to the value of the capacitance is necessary to account for the circular shape of the EE depletion region, consisting in a new term in (6), which involves a second EE parameter D_2 [18]. The value of D_2 (0.34 if no surface effect is considered) has in turn to be modified also by the effect of

V_S in a factor $[\beta(V_S)/\beta_0]^2$ (the square exponent appears when integrating (6) in a circular geometry).

As a result, extending the model proposed in [18] to the case of a general shape and considering surface effects, the absolute capacitance of a PSBD can be calculated as

$$C_T(V) = A\frac{\varepsilon_{sc}}{W(V)} + L_{\text{Contour}} 2D_1 \frac{\beta(V_S)}{\beta_0}\varepsilon_{sc} + 3D_2\left[\frac{\beta(V_S)}{\beta_0}\right]^2 \varepsilon_{sc} W(V) \text{ (in } F) \quad (7)$$

with

$$\frac{\beta(V_S)}{\beta_0} = 1 + 0.300 \cdot V_S + 0.146 \cdot V_S^2$$

which is the result of the addition of the ideal parallel-plate term (proportional to the area of the anode, A), the EE term (proportional to the length of the contour of the anode, L_{Contour}, and independent of the epilayer doping) and a third term associated to the circular sections of the EE depletion region (independent of the anode geometry but dependent on the biasing and epilayer doping, as it is proportional to W). Notice that circular sectors are not only present in the depletion region of circular anodes, but also at the corners of rectangular ones, and their contribution to the total capacitance is not accounted for by the first two terms in (7). Therefore, the third term must be included even in the case of rectangular geometries. Indeed, such a term does not contain any dependence on characteristic parameters of a circular geometry. The third contribution to the capacitance is not present in our MC simulations, since the 2-D approach implies homogeneity in the nonsimulated dimension, and therefore absence of any circular section in the EE depletion region in such a direction.

IV. Conclusion

By means of 2-D MC simulations of PSBDs, we have analyzed the deviations of the internal charge variation and the associate intrinsic capacitance with respect to the ideal 1-D behavior. The 2-D shape of the depletion region beneath the Schottky anode leads to an excess of depleted charge (EE), which increases linearly with respect to the reverse applied voltage, thus contributing with a constant term to the global capacitance of the PSBD (characterized by an EE parameter, β), which is proportional to the length of the contour of the anode but independent of the doping level of the epilayer. By modeling the surface charges at the epilayer–dielectric interface (characterized by the value of its surface potential V_S), we have evidenced a dependence of β on V_S, leading to a reduction up to a 15% from its nominal value β_0 (with a dependence that can be approximated by a second-order polynomial equation). The compact model provided by the analytical (5) and (7) can be easily implemented in LEC-HB simulators (with correct values of the series resistance obtained with a 2-D current model) for an accurate prediction of the diode response in multiplying applications up to, at least, 300-GHz LO input signal [18].

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