# STATE -OF-THE-ART PERFORMANCE OF A HETEROSTRUCTURE BARRIER VARACTOR TRIPLER OPERATING AT 250 GHz

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***Abstract* — Record performances were demonstrated in terms of output power (>9 mW) and conversion efficiency (12%) for a 250 GHz Heterostructure Barrier Varactor tripler. These excellent performances can be explained by the highly non linear capacitance-voltage characteristics of InGaAs/InAlAs/AlAs diodes having a zero-bias capacitance of 1fF/μm$^2$, a capacitance ratio of 6:1 and a breakdown voltage of 12 V.**

## I. INTRODUCTION

The Heterostructure Barrier Varactor (HBV) exhibits a sharp non linearity and a symmetrical Capacitance-Voltage (C-V) characteristic about zero volt. These properties greatly enhance the functionality of the devices since only odd harmonics are generated. Also, several degrees of freedom are afforded by the use of semiconductor heterojunctions. Another important advantage stems from the fact that the devices can be vertically stacked during epitaxy. This epitaxial integration opens the way for high-voltage low-capacitance devices. HBV triplers with 2mW and up to 5% have been achieved which operate between 210 and 280 GHz using a whisker contact technology [1]. A 200 GHz tripler using a GaAs single barrier whisker-contacted varactor with an overall efficiency of 2 % was demonstrated at the Jet Propulsion Laboratory [2]. Output power of 3.6mW (2.5% conversion efficiency) was published at 234 GHz using AlGaAs/GaAs heterostructures [3]. Recently, we published 5 % efficiency and 5mW output power at 216 GHz [4]. In the present work, we report record performances in terms of maximum efficiency (12.3 %) and output power (in excess of 9 mW) at 247.5 GHz. To our knowledge, these are the highest results at the time of writing.

## II DIODE DESIGN AND FABRICATION

The HBV devices are fabricated at the University of Lille using an Indium Phosphide technology. Basically this technology has a number of practical advantages over its GaAs-based counterpart. First-of all, pseudomorphic growth of step-like InGaAs/InAlAs/AlAs barrier enables the voltage handling to be dramatically improved (by a factor of 3) due to a more efficient blocking barrier [5]. The apparent barrier is about 600meV (tunneling through the barrier) whereas it is ~ 180meV for GaAs/$Al_{0.7}Ga_{0.3}As$/GaAs HBV's. In addition, the narrow gap of the cladding and contact layers is a welcome feature for very high frequency operation notably through a decrease of series resistance. These are the primary reasons of the very good performances reported here with respect to early work using GaAs devices operating in this frequency range.

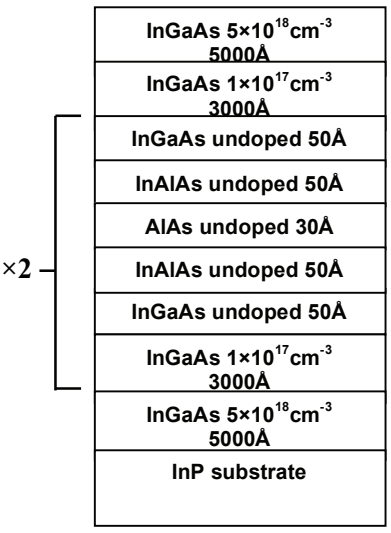


Fig. 1: MBE growth parameters for dual barrier heterostructures

Figure 1 shows the growth sequence of the fabricated devices. Starting from an InP Semi-insulating substrate, we first grew a buried highly doped layer. The doping concentration is here essential since most of the series resistance is due to the spreading of current lines at this location. The cladding InGaAs layer, where the capacitance modulation takes place, have a typical thickness of 300 nm for a doping level of 1x 10 $^{17}$ cm$^{-3}$. The guide lines for this choice are the minimization of current saturation effects which can be overcome by a quite high doping concentration. We preferred to limit the

thickness of the barrier for enhancing the capacitance contrast as seen in the following. At last a highly doped capping layer enables us to lower the contact resistance.

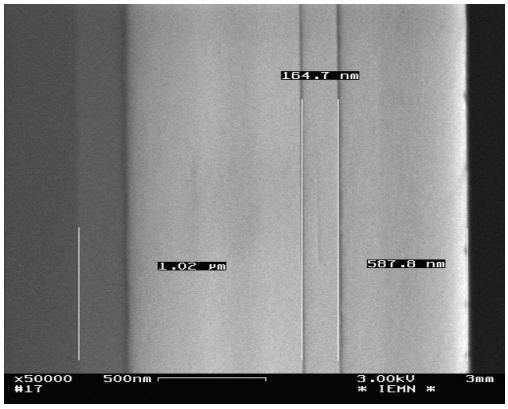


Fig. 2 Scanning Electron Micrograph of a Dual Barrier Heterostructure

Confidence into the quality of epitaxial stacking can be achieved by characterizing the samples via the slice, as seen in figure 2, by means of a scanning electron analysis. The two barrier appear in this photo in dark.

The devices, with two barriers stacked during the same epitaxy, were subsequently planar integrated with coaxial-, coplanar-and strip-type configurations. The various types of configuration can be recognized in Figure 3 which shows a SEM view of the set of devices. The coaxial-type is used for current-voltage and capacitance-voltage assessments without the requirement of an air bridge technology and of de-embedding techniques [6]. On the other hand such a configuration can be used to rf characterize the device up to the pump frequency ~85 GHz in the present work. On this basis, Figure 4 shows the typical capacitance-voltage characteristics for a Dual Barrier Heterostructure Barrier Varactor (DHBV). A highly symmetrical profile is observed, this is an essential characteristic for tripling or quintupling applications at high frequency. A zero bias capacitance of 1fF/µm$^2$ with a capacitance ratio of ~6:1 was observed. Also, no degradation was found versus frequency. The high degree of symmetry enables the second harmonic to be readily rejected.

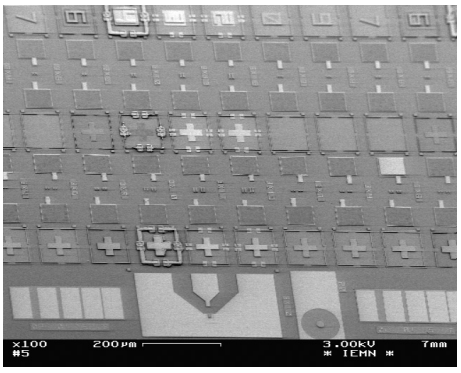


Fig. 3: SEM view of the mask set including coaxial, coplanar and microstrip type configurations

From dc measurements, it was also found that the leakage conductance is less than 100 nS/µm$^2$ up to 10 V. Such a low level of spurious conduction through the barrier is of prime importance for subsequent large signal operating conditions. Indeed, for low quality factor devices a significant degradation of device performance is observed due to the so called self heating effect [3].The non upconverted power increases the diode temperature with a subsequent decrease in conversion efficiency. Such effects are alleviated for the present technology since the shunt conductance level remains negligible with respect to the susceptance at increasing temperature.

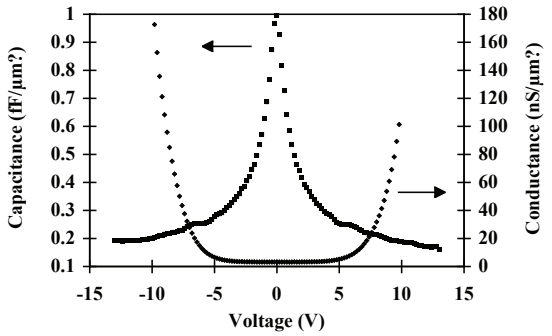


Fig. 4 C-V and G-V characteristics of a dual barrier device measured at room temperature

## III DEVICE INTEGRATION AND SMALL SIGNAL RF MEASUREMENTS

In view of tripler experiments, the diodes have been planar integrated and contacted by means of air bridges. Further details about the technological procedure can be found elsewhere[4]-[6]. The next stage in the diode characterization was to measure the embedding elements. To this aim, a coplanar waveguide configuration was employed for probing the devices at the wafer level. In practice the self-inductance, due to the interconnecting elements, resonates with the diode capacitance and hence a well defined resonant effect can be pointed out by measuring the small signal impedance of diodes over a broad frequency range. Figure 5 illustrates such experiments carried out up to 110 GHz, by varying either the diode area and/or the bias voltage.

By fitting these admittance variations against frequency by means of an equivalent circuit within the broad measurement bandwidth, a lumped-element circuit can be derived with accuracy. Notably we can measure the series resistance which is one of the key parameter in the frequency capability of the devices. We thus found 3.8 Ω for a 30µm$^2$ (Fc= 2.1 THz), 2.5 Ω for a 60 µm$^2$ (Fc= 1.5 THz) and 2.2 Ω for 121 µm$^2$ (Fc= 1.2 THz). Also the determination of such a small signal equivalent circuit permits us to carry out some harmonic balance simulation in order to predict the conversion efficiency and the expected output power for a tripling operation with an output frequency of 250 GHz. In these simulations, the fact to include or not the extrinsic elements modifies, as

expected, the optimum source and load impedances since no extra resistive term was added.

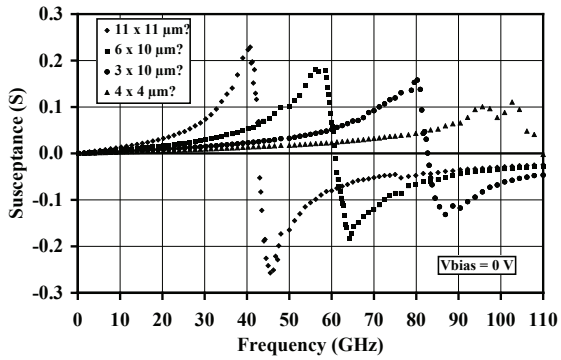


Fig. 5: Small signal susceptance versus frequency. A well defined resonance can be followed as a function of diode area or bias voltage

The third test scheme was dedicated to the large signal experiments in tripler blocks. In that case the samples consisted of two pads facing each other with the devices further integrated in series by means of air bridges. Figure 6 (a) and (b) show Scanning Electron Microphotographs of this kind of devices. In order to reduce the parasitic resistance, which is dominated by the spreading resistance, we used a finger- shaped configuration. Deep etch was also developed with the aim to reduce the parasitic capacitance but faces, for this specific batch, the problem of undercutting effects. The last stage in the device fabrication was to thin the substrate by chemical etching down to 35 µm in the best case and to dice the samples into discrete devices. The overall lateral dimensions were typically 200x 100 $\mu m^2$.

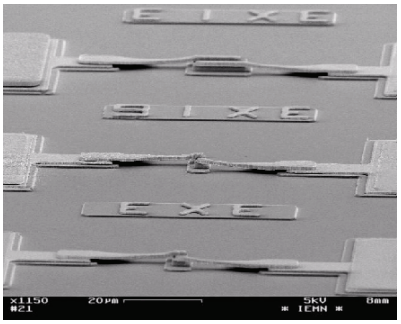

Fig. 6 (a) Scanning Electron micrograph illustrating the planar integration of the devices

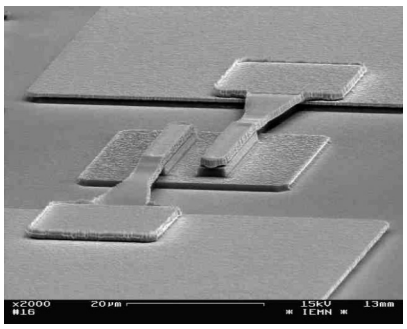

Figure 6(b) close-up SEM view of intregrated devices

## IV TRIPLER DESIGN AND MEASUREMENT

The multiplier block used for the tripler measurement at 250 GHz is shown in Figure 7. It is a crossed wave guide type mount, designed and manufactured by Matra Marconi Space by making use of space qualified materials and processes. The design is a similar fashion to that proposed by Archer [7]. The pump power incident in the full-height WR-10 wave-guide is fed to the planar integrated diode through a stripline E-plane transition and through a low pass filter implemented on a 75 µm-thick fused silica substrate. Impedance matching at the pump power is achieved using two sliding non contacting backshorts. The output is also equipped with two backshorts. This tuning configuration with two degrees of freedom facilitates the matching of the optimum embedding impedances calculated as aforementioned by harmonic balance analysis. The strip line low-pass filter is a five sections Chebytcheff design implemented by using alternate high-low pass impedance strip line sections printed on the fused silica substrate. The diode chip is mounted in a flip-chip technology. Prior to the fabrication some of the block elements were simulated by means of the High Frequency Structure Simulator (HFSS ) by HP. Sliding the two backshort independently on both output and input ports enables to meet the optimum impedances. In contrast this solution employing four tuning elements can increase the loss term in the non contacting backshorts. Also the radiation pattern in both input and output waveguides was studied along with the filtering section which exhibits a low loss at the pump power (@83 GHz) and a good rejection @250 GHz

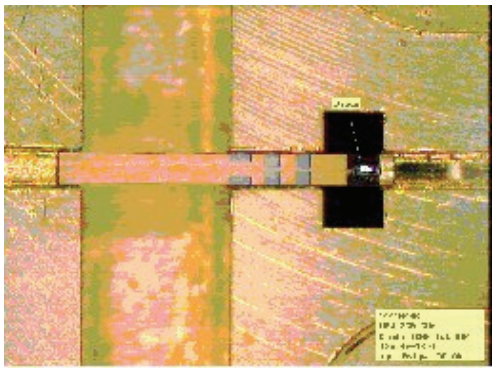

Fig. 7 Tripler block designed by Matra Marconi Space Toulouse

In the first experiments, which were performed at a moderate source power, the input power was delivered by a Gunn oscillator which can be mechanically tuned for output frequency between 248-253 GHz. Input power was measured with a HP power head which was recently calibrated whereas output power was recorded using an Anritsu power head with comparison with a Thomas Keating power meter. Recently the accuracy of the absolute power measurements were also checked by tests at Millilab in Finland. Figure 8 shows the frequency dependence of the performance of the devices achieved under these conditions.

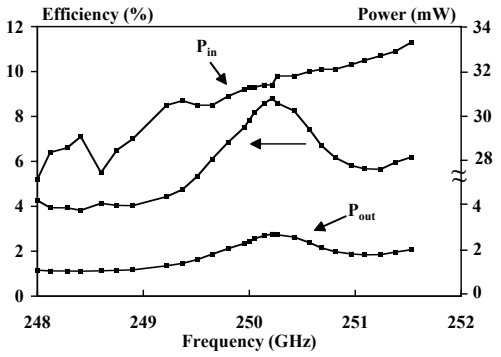


Fig. 8.Input and Output power along with conversion efficiency versus frequency. The diode diameter is 6µm. The number of barrier is four

For experiments at higher power levels, performed at Ecole Normale Supérieure (ENS) notably up to Pin = 100 mW, we used a Thomson CSF carcinotron which can deliver a much higher power in the 77-82.25 GHz frequency range. Figure 9 shows the variations of the output power and conversion efficiency as a function of input power for an output frequency of 247.5 GHz. Tuning was adjusted for better performance at a pump power of 50 mW. This backshort tuning was maintained at a constant level for recording the variations illustrated in Figure 9. The maximum efficiency typically occurs for pump powers of approximately 60 mW. The maximum output power was 9.5 dBm and was obtained with an efficiency of 10.5 %. On the other hand, second harmonic rejection was measured and found to be -25 dB below the third harmonic which is a consequence of the excellent symmetry in the C-V characteristics.

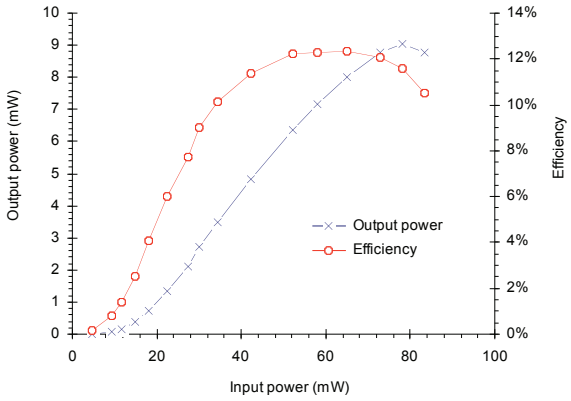


Figure 9 Output power and efficiency versus input power.

Further improvements in the performances not only in terms of power output but also in frequency capability can be expected on the basis of several improvements. First of all it can be seen that the loss in the block could be optimized at short term by a careful optimization of the sliding tuning elements. Also the matching of the diode to the external circuit could be improved. It seems however that a full ElectroMagnetic (EM) analysis is necessary for that purpose. Preliminary EM simulations of the environment of the integrated diodes were already performed using an extra port for including the diode in the EM simulation domain. A full analysis with an internal port to couple circuit analysis (MDS) and EM analysis (HFSS) should be better in essence. On the other hand the power capability of the devices could be greatly increased by stacking more barrier in series. So far we succeeded in a eight barrier scheme. It can be shown that the power can be multiplied by a factor $n^2$ where n is the number of basic heterostructures provided the impedance is kept constant. Nevertheless the need for driving the diodes in non linear regime becomes more stringent. At last the diodes itself could be further optimized by means of a prewell and postwell configuration. Recently it was shown that such a band gap engineering permits to narrow the voltage range for non linear behavior while preserving a high capacitance ratio

## V CONCLUSION

We have achieved record performances with InP-based HBV's which have been fabricated in stacked and integrated planar configurations. An efficiency in excess of 10 % and around 10 dBm output power have been demonstrated at 250 GHz. We believe that further improvements in these values can be achieved by increasing the integration level. Preliminary experiments show voltage handling as high as 50 V with a zero-bias capacitance level $C_{J0}$=250 aF/µm$^2$ with eight barriers.

## VI ACKNOWLEDGMENTS

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