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Record performance of a 250GHz InP-based heterostructure barrier varactor tripler

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Record performances in terms of output power (9.5dBm) and maximum efficiency (12.3%) have been demonstrated for a 250GHz heterostructure barrier varactor tripler. Such good results are explained by the use of highly nonlinear InGaAs/InAlAs/AlAs planar integrated diodes, which are seen to have numerous advantages over their GaAs-based counterparts.

Introduction: Heterostructure barrier varactors (HBVs) exhibit a symmetrical capacitance-voltage (C-V) characteristic with a sharp nonlinearity which make them attractive for power up-conversion using odd harmonics only. An output power of 3.6mW (2.5% conversion efficiency) at 234GHz using AlGaAs/GaAs heterostructures was recently published [1]. 5% efficiency and 5mW output power at 216GHz from InGaAs/InAlAs/AlAs heterostructures have also been reported [2]. In this Letter, state-of-the art performances with 12.3% maximum efficiency and 9.5dBm output power have been achieved from InP-based HBVs planar diodes using a waveguide tripler block at ~250GHz. These results are the highest performances to date for HBV multipliers operating at these frequencies.

Diode design and fabrication: The HBV devices are fabricated at the University of Lille in France using indium phosphide technology, which has a number of practical advantages [3]. Notably, the pseudomorphic growth of a step-like InGaAs/InAlAs/AlAs barrier enables the voltage handling to be dramatically improved due to a more efficient blocking barrier. As a consequence, the so-called self-heating effects can be overcome. In addition, the narrow gap of the cladding and contact layers is an advantageous feature for very high frequency operation, notably by alleviating saturation current effects at moderate doping levels. These are the primary reasons for the very good performances reported here with respect to early work using GaAs devices operating in this frequency range.

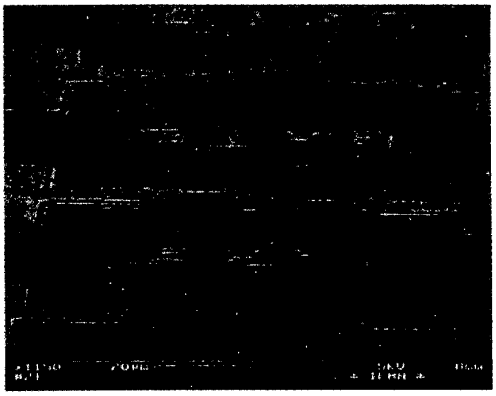

Fig. 1 *Scanning electron microphotograph of devices vertically stacked (during epitaxy) and laterally series integrated (by means of air bridges)*

The devices, with two barriers stacked during the same epitaxy, were connected by means of air bridge techniques to produce two laterally integrated diodes in series. Fig. 1 shows a scanning electron microphotograph of typical devices which have the equivalent of four barriers in series. Their fabrication by means of a set of eight masks involves optical and electron beam lithography for patterning, reactive ion etching for mesa fabrication, sequential evaporation for ohmic contact material deposition and air bridge implementation along with electroplating for pad metal overlay.

The capacitance (C-V) and conductance (G-V) characteristics against applied voltage are shown in Fig. 2 for a dual barrier configuration. These small signal impedance measurements were performed using a coaxial type configuration to assess the epitaxy quality and with a coplanar waveguide scheme for characterising the diode embedding [4]. The C(V) is highly symmetric, demonstrating a capacitance ratio of 6:1. The zero bias capacitance is 1 fF/μm² for two barriers in series and scales with layer complexity. This high degree of symmetry enables the second harmonic to be readily rejected. The leakage conductance is seen to be < 100nS/μm² (up to 10V).

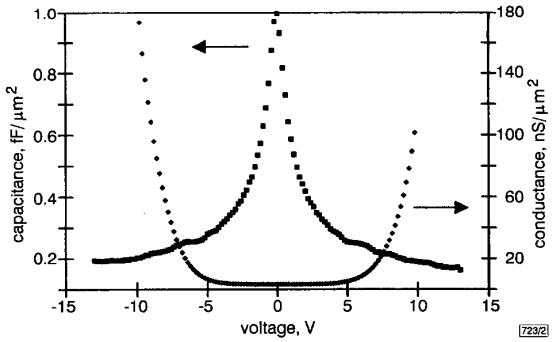

Fig. 2 *Small signal conductance and capacitance against voltage for dual barrier configuration*

Tripler measurement: The multiplier block used for the tripler measurement at 250GHz is a crossed waveguide type mount, designed and manufactured by Matra Marconi Space, making use of space qualified materials and processing. The pump power, which is incident in the full-height WR-10 waveguide, is fed to the planar integrated diode through a stripline E-plane transition and through a Tchebichev lowpass filter implemented on a 75μm thick fused silica substrate. Impedance matching at the input and output terminals is achieved using two sliding noncontacting backshorts for each port. The diode chip is mounted in a flip-chip technology after lapping and dicing the wafer into discrete chips, which have dimensions of 100 × 220μm² and a thickness up to 30μm.

Tripler experiments were performed at Observatoire de Paris and Ecole Normale Supérieure. The output power was measured with an Anritsu power head in comparison with a Thomas Keating power meter. For these experiments, at a relatively high power of up to P_{in} = 100mW, we used a Thomson CSF carcinotron in the 77–82.25GHz frequency range. Fig. 3 shows the variations in output power and conversion efficiency against input power for an output frequency of 247.5GHz. The maximum efficiency (12.3%) typically occurs for pump powers of ~60mW. The maximum output power was 9.5dBm and was obtained with an efficiency of 10.5%.

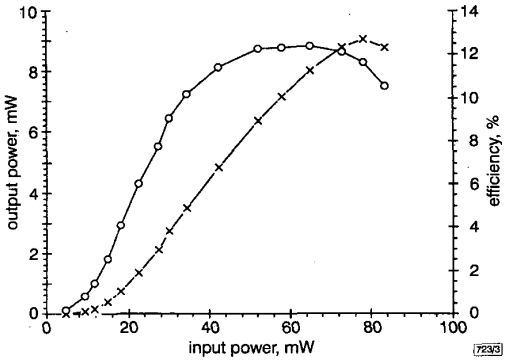

Fig. 3 *Output power and efficiency against input power for four barrier device (diameter 6 μm)*

—X— output power
—O— efficiency

Conclusion: We have achieved the highest output power and conversion efficiency reported to date for heterostructure varactor triplers by utilising InP-based highly nonlinear devices. We believe that further improvements in these values can be achieved by increasing the integration level. Preliminary experiments show voltage handling as high as 40V with a zero-bias capacitance level C_{j0} = 250aF/μm² when eight barriers are integrated in series.

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Chaos synchronisation in high-order circuits and time-delay systems using observer

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An observer-based technique is described for the synchronisation of complex chaotic dynamics, generated by systems with several positive Lyapunov exponents. The tool is used to synchronise, via a scalar signal, a recent example of an eighth order circuit and a cell equation in a delayed cellular neural network.

Introduction: In the preceeding decade strong interest has been generated into the study of synchronisation in chaotic circuits, due to the potential application to communication systems. In particular, the challenge is to synchronise, via a scalar signal, very complex chaotic dynamics, generated by systems with several positive Lyapunov exponents [1 – 3].

In this Letter we focus on the chaotic synchronisation of both high-order circuits and time-delay systems. A unified tool, based on a linear observer, is described and applied to synchronise, via a scalar signal, a recent example of an eighth order circuit [3] and a cell equation in a delayed cellular neural networks [4].

Synchronisation tool: Let the chaotic drive system be described by the following state and output equations, respectively:

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{b}f(\mathbf{x}(t-\tau)) \quad y(t) = \mathbf{k}\mathbf{x}(t) + f(\mathbf{x}(t-\tau)) \tag{1}$$

where $\mathbf{x} \in \Re^n$ is the state, $y \in \Re$ is the scalar output, f: $\Re^n \rightarrow \Re$ is a nonlinear vector field, $\tau \in \Re^+$ is the delay, $\mathbf{A} \in \Re^{n\times n}$, $\mathbf{b} \in \Re^{n\times 1}$ are known parameters, whereas $\mathbf{k} = [k_1, k_2, ..., k_n] \in \Re^{1\times n}$ will be determined later on. The observer-based techniques enable the state $\mathbf{x}(t)$ to be reconstructed by the response system using measurements of the observed quantity $y(t)$ [1]. Since the response system need not be a copy of the drive system in order to obtain synchronised dynamics [1], in this Letter its state and output equations are considered in the following form:

$$\dot{\hat{\mathbf{x}}}(t) = \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{b}(y(t) - \hat{y}(t)) \qquad \hat{y}(t) = \mathbf{k}\hat{\mathbf{x}}(t) \tag{2}$$

where $\hat{y}(t)$ is the observer prediction of the received signal $y(t)$. This leads to the error system given by $\dot{\mathbf{e}}(t) = \mathbf{A}\mathbf{e}(t) - \mathbf{b}\mathbf{k}\mathbf{e}(t)$, with $\mathbf{e}(t) = (\hat{\mathbf{x}}(t) - \mathbf{x}(t))$, which can be globally asymptotically stabilised at the origin by proper $\mathbf{k}$ if the controllability matrix is full rank [1]. Note that the proposed tool extends the results in [2] to time-delay systems. Moreover, it exploits a *linear* observer, whereas the approach in [2] is based on a *nonlinear* observer.

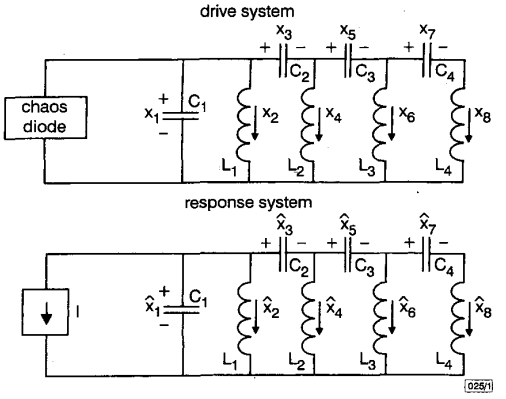

Fig. 1 *Synchronisation scheme*

Drive system includes chaos-diode whereas response system is linear observer

Synchronisation of eighth order circuits: The high-order circuit family recently proposed in [3] contains a novel two-terminal device, called a chaos-diode (χ–diode), which includes both a negative impedance converter and a Schmitt trigger. The example eighth order circuit is reported in Fig. 1. The current-voltage characteristic of the chaos-diode is given by $\lfloor 4.2 s_j\ (x_1, s_{j-1}) - 0.6x_1 \rfloor$, where $s_j = H(x_1 - 1 + 0.9s_{j-1})$, $j = 1, 2, ...$, is the discrete-state func-