200, 400 and 800 GHz Schottky Diode "Substrateless" Multipliers: Design and Results

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Abstract — Several sub-millimeter doubler circuits have been designed and built using a new fabrication technology. To reduce the RF losses in the passive circuitry, the substrate under the transmission lines is etched away, leaving the metal suspended in air held by its edges on a GaAs frame. This allows the circuit to be handled and mounted easily, and makes it very robust. To demonstrate this technology, broadband balanced planar doublers have been built and tested at 400 GHz. The next generation 200, 400 and 800 GHz doublers with improved performance will also be discussed. The 368-424 GHz circuits were measured and achieved 20% efficiency at 387 GHz. The 3-dB bandwidth of the fix-tuned doubler is around 9%. The maximum output power measured is around 8 mW and drops down to 1mW at 417 GHz. This represents the highest frequency waveguide based planar doubler to date in the literature.

I. INTRODUCTION

Currently there is a demand for a large quantity of readily fabricated and assembled wide-bandwidth frequency multiplier chains [1-3] for use in sub-millimeter wave heterodyne receivers. These space-borne radiometers are primarily intended for astrophysical observation. The Jet Propulsion Laboratory maintains a concentrated effort to develop and implement novel technologies to produce robust, reliable and repeatable planar Schottky diode multipliers for these applications [4]. This paper will focus on the "substrateless" technology that has been developed, which has made possible construction of state-of-the-art multipliers in the 400 GHz range. The design methodology and its interaction with the technology will be discussed. Based on the lessons learned during the first demonstration, the next generation of multipliers has been designed to improve performance, and will be briefly discussed.

II. DESIGN PHILOSOPHY

The multipliers each consist of two components – nonlinear solid state devices (Schottky diodes) and the surrounding input, output and impedance matching circuitry. The diodes are integrated with metallic circuitry using a GaAs MMIC process. Additional passive circuitry is incorporated in waveguide. The lines fabricated on GaAs have the dual roles as waveguide transitions and as part of the impedance matching. After much experimentation, we now keep the majority of the impedance matching in the waveguide to take advantage of its low-loss performance. Since the diodes have a high Q, circuitry near the diodes can be used to tune out some of their reactance.

All of the doublers use the balanced planar diode configuration [5,6]. Balanced doublers incorporate symmetrical pairs of diodes configured so that they only respond to odd harmonics at the input and even harmonics at the output, making it easier to separate the frequencies and facilitate the design process.

III. "SUBSTRATELESS" TECHNIQUE

To reduce the losses in the metal lines fabricated on GaAs and to facilitate the design JPL has demonstrated a new technology that can work up to the THz range [4,7,8]. This technology relies on standard processing techniques to fabricate the diode structures and metal lines on the front side of the wafer. During back-side processing the wafer is patterned and etched to remove GaAs from under most of the transmission line metal, leaving the lines suspended in air from a GaAs frame, shown in Figure 1. The Schottky diodes sit on one edge of this frame resulting in a "substrateless" structure monolithically incorporating both the active devices and the close-in metallic circuitry.

There are several advantages to the substrateless technology. Without the semiconductor underneath the lines, a wider line is required to give a specific impedance, so both conductive and dielectric loss is reduced. Lack of

dielectric aids in preventing multimoding, which would otherwise be exacerbated by the presence of GaAs. This permits a much more flexible design procedure. The structure is physically much larger than previous diode chips allowing easier handling and mounting, while at the same time allowing the diodes to be precisely aligned with the most critical circuitry. Beam leads placed on the structure improve heat transfer and simplify the assembly procedure when mounting in the waveguide block. Since the beam leads lie directly on the block or bias chip capacitor, no wire bonding, soldering or epoxy attachment is needed. The circuit is mounted to the block with the devices facing up which facilitates inspection during assembly. Electrically, the beam leads serve as grounding lines to the block and as the waveguide transitions.

The primary limitations to extending this technology to higher frequencies are the error tolerances in positioning the diodes on the frame, and the frame itself, which lies in the output matching circuitry and waveguide. Many simulations have shown that having the frame in the output guide does not substantially effect either the propagation in the guide or the coupling from diodes to the guide. However, the dimensions of the output circuitry and frame must be carefully tailored to prevent waveguides modes other than the TEM mode from leaking between the diodes and the output guide. This would adversely affect the performance of the output circuit.

IV. Design Methodology

The multipliers are designed using a three-step process. First, a non-linear circuit simulator and a diode model implementation developed at JPL are used to optimize the dimensions, doping profile, and number of diodes to be used in the circuit. This calculation also determines the diode junction characteristics and embedding impedances that give the best performance.

Second, the multiplier input and output matching circuits are synthesized using an electromagnetic (EM) finite-element simulator to calculate their S-parameters in an iterative procedure. To simplify and speed up the process, the passive circuitry is divided into individual elements giving several S-parameter matrices. These are entered into a linear simulator along with the diode impedances calculated using the non-linear simulator. Most of the impedance matching is accomplished using waveguide and stripline which can be accurately represented in the linear simulator, simplifying their optimization. Much use is made of the symmetries of the balanced doubler to speed up the design further.

Finally, the diode non-linear models and the EM simulator S-parameter matrices of the complete passive circuits are recombined in the non-linear simulator to determine the overall performance.

The 200, 400 and 800 GHz doublers are designed to operate with input powers of 200 mW, 50 mW and 7 mW respectively and incorporating six, four and two diode arrays to handle the power.

A sketch of the original 400 GHz doubler whose measured performance is described below appears in Figure 1, along with the new design. The new designs are simpler, and transfer most of the impedance matching to the waveguide rather than the GaAs circuit. The second difference is that the large low-pass filter at the right, used for DC bias bypass, is replaced with a much smaller integrated Si_3N_4 capacitor. The metal lines near the diodes are open stubs helping to cancel the inductance of the diode structure at the output frequency. The output signal travels through the channel from the input guide to the output guide. The circuit symmetry prevents the input frequency from leaking into the output and also prevents the output signal from leaking into the input, as long as the reduced height input guide is cut off for the TM_{11} mode. The line extending across the output waveguide is an E-field probe that goes through the integrated capacitor to a beam lead attached to a chip capacitor as an insulated stand-off. The 200 GHz design dispensed with the integrated capacitor and uses the chip capacitor alone. The diodes are grounded to the waveguide block with the two beam leads at the left.

V. 400 GHz Results

Figure 2 shows the original 400 GHz doubler mounted in a block. For testing, a BWO and power combined MMIC amplifiers were used to deliver about 250 mW at 100 GHz to the multiplier chain, and the output is measured using a calibrated Keating meter as well as a University of Massachusetts wideband calorimeter [7,8].

An example of the performance of one the 400 GHz doublers appears in Figure 3. The efficiency varies between 10 and 20 % over the lower half of the band, with output power of 5 to 8 mW. Figures 4 through 6 show the estimated performance of the improved 200, 400 and 800 GHz doublers. These are calculated efficiencies, and the actual measured performance may be reduced due to machining and processing variations, and deviations of the diode performance from the model used. In future designs an improved diode model will be incorporated that better accounts for the diode physics, especially temperature effects.

VI. Conclusions

State-of-the-art multiplier performance using a new technology has been demonstrated in the 400 GHz range. This "substrateless" technology integrates air-dielectric transmission lines and beam leads with Schottky diodes to achieve good performance in the sub-millimeter wave range. Peak efficiency of 20% for a balanced doubler with 8 mW of output power has been measured at 387 GHz. This technique promises to simplify planar multiplier design up to one THz. Next generation designs for 200, 400 and 800 GHz are presented and discussed.

Acknowledgments

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REFERENCES

[1] E. F. van Dishoek and F. P. Helmich, "Scientific drivers for future high-resolution far-infrared spectroscopy in space," *Proc. 30th ESLAB Symp., Submillimetre and Far-Infrared Space Instrumentation 1996*, ed. E. J. Rolfe, ESA SP-388, pp. 3-12.

[2] G. Pilbratt, "The FIRST mission," *Proc. ESA Symp., The Far Infrared and Submillimetre Universe 1997,* ESA SP-401.

[3] N. D. Whyborn, "The HIFI Heterodyne Instrument for FIRST: Capabilities and Performance," *Proc. ESA Symp, The Far Infrared and Submillimetre Universe 1997,* ESA SP-401.

[4] I. Mehdi, E. Schlecht, A. Arzumanyan, J. Bruston, P. Siegel, R. Peter Smith, J. Pearson, S. Martin and D. Porterfield, "Development of millimeter and submillimeter-wave local oscillator circuits for a space telescope," *Proc. SPIE*, vol. 3795, pp. 329-337, *Terahertz and Gigahertz Photonics,* R.J. Hwu, K. Wu, Eds., October 1999.

[5] Rizzi, B.J., Crowe, T.W., Erickson, N.R., "A High-Power Millimeter-Wave Frequency Doubler Using a Planar Diode Array," *IEEE Microwave Guided Wave Lett*., vol.3, pp. 188-190, June 1993.

[6] N.R. Erickson, "Diode Frequency Multipliers for Terahertz Local Oscillator Applications," *Proc. SPIE*, vol. 3357, pp. 75-84, *Advanced Technology MMW, Radio, and Terahertz Telescopes*, T.G. Phillips, Ed., July 1998.

[7] E. Schlecht, J. Bruston, A. Maestrini, S. Martin, D. Pukala, R. Tsang, A. Fung, R. P. Smith, and I. Mehdi, "200 and 400 Ghz Schottky diode multipliers fabricated with integrated air-dielectric 'substrateless' circuitry," *Eleventh International Symposium on Space Terahertz Technology*, Ann Arbor, May 2000.

[8] A. Maestrini, D. Pukala, F. Maiwald, E. Schlecht, G. Chattopadhyay, and I. Mehdi, "Cryogenic operation of GaAs based multiplier chains to 400 GHz, " *Eighth International Terahertz Conference*, Darmstadt, Germany, September 2000.

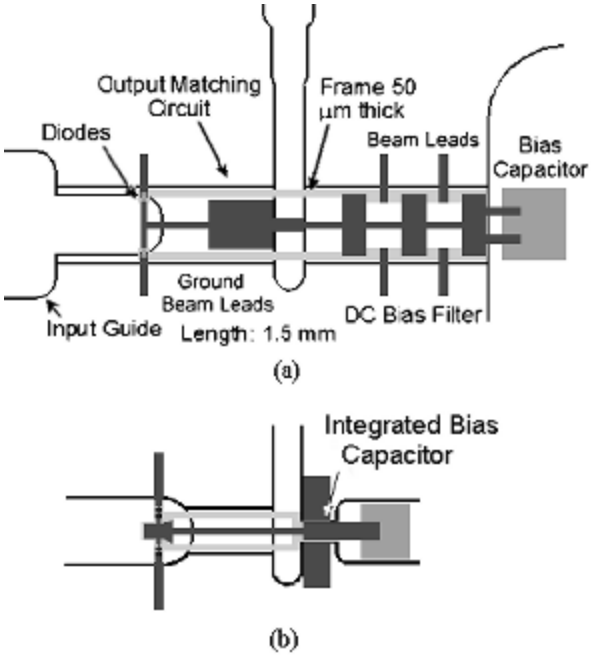

Figure 1. 400 GHz doublers. (a) Original. (b) Next generation.

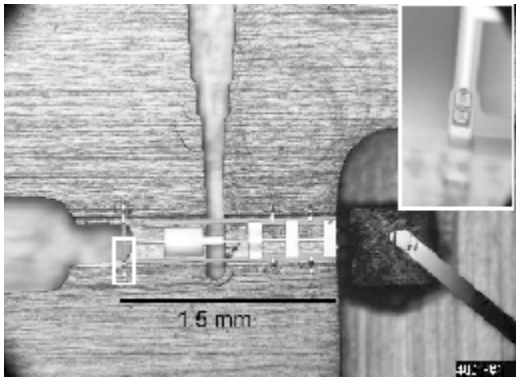

Figure 2. 400 GHz doubler in block. Inset shows diodes on frame.

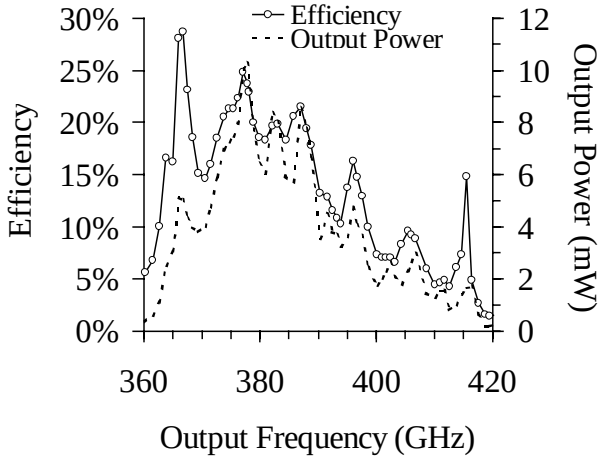

Figure 3. Measured efficiency , output and input power of 400 GHz doubler.

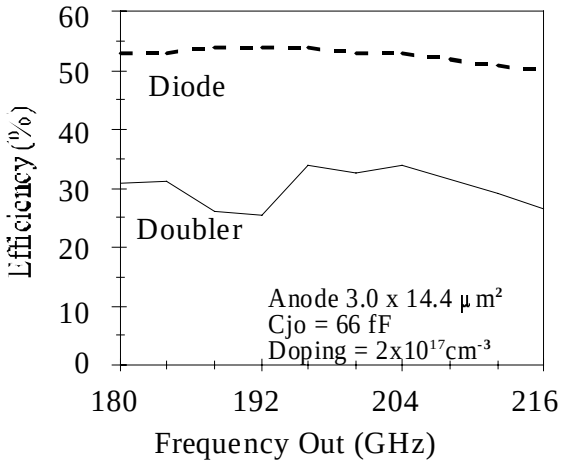

Figure 4. Calculated efficiency of new 200 GHz doubler.

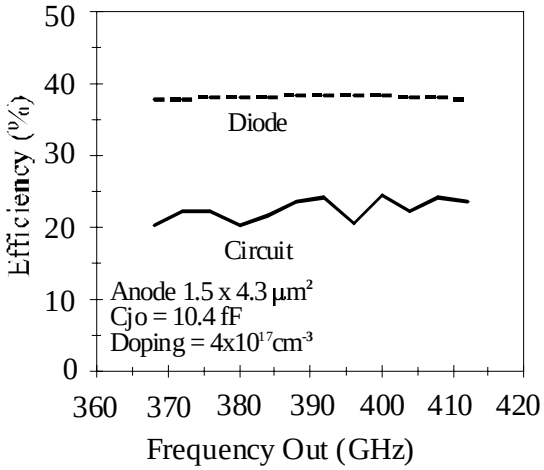

Figure 4. Calculated efficiency of new 400 GHz doubler.

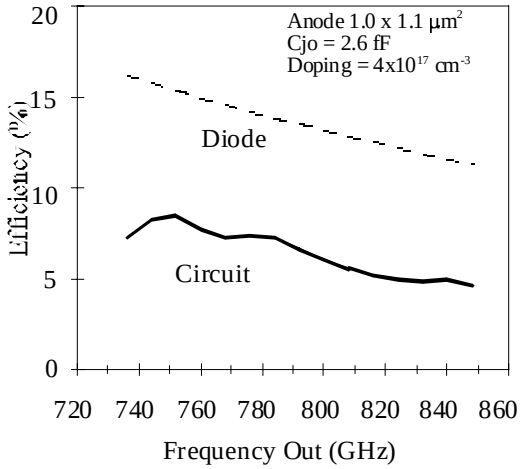

Figure 6. Calculated efficiency of new 800 GHz doubler.