

A Frequency-Multiplied Source With More Than 1 mW of Power Across the 840–900-GHz Band

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Abstract—We report on the design, fabrication, and characterization of an 840–900-GHz frequency multiplier chain that delivers more than 1 mW across the band at room temperature with a record peak power of 1.4 mW at 875 GHz. When cooled to 120 K, the chain delivers up to 2 mW at 882 GHz. The chain consists of a power amplifier module that drives two cascaded frequency triplers. This unprecedented output power from an electronic source is achieved by utilizing in-phase power-combining techniques. The first stage tripler uses four power-combined chips while the last stage tripler utilizes two power-combined chips. The source output was analyzed with a Fourier transform spectrometer to verify signal purity.

Index Terms—Frequency multiplier, frequency tripler, local oscillator, planar diode, power combining, Schottky diode, submillimeter wavelengths, varactor.

I. INTRODUCTION

LACK OF tunable, broadband, robust, and reliable power sources in the submillimeter-wave frequency range has been a major limiting factor in developing applications in this part of the spectrum. The range from 0.3 THz, where transistors show only limited gain, to about 10 THz, where solid-state lasers become available, continues to be of significant scientific interest where sources are much needed [1]–[4]. Photonic solutions to coherent generation at terahertz frequencies have dominated the field for decades starting with far-infrared lasers able to produce tens of milliwatts of coherent power, to femtosecond infrared lasers and photoconductors that enable broadband terahertz sources suited for numerous spectro-imagery applications [5]. Photomixers are also an attractive solution for generating coherent terahertz continuous waves (CWs) thanks to their wide frequency tunability [6], [7]. Recently, quantum

cascade lasers have made incursions into the sub-terahertz domain and are routinely delivering milliwatts or tens of milliwatts in the 1–4-THz range [8], [9] albeit at cryogenic temperatures and with limited bandwidth. These lasers have been successfully phase locked and used to build the local oscillator of a heterodyne receiver based on a super-conducting hot-electron-bolometer (HEB) mixer working at 2.8 THz [10].

In contrast, electronic sources in the terahertz region are scarce; if we put aside non solid-state sources like the power-hungry and heavy backward-wave oscillators (BWOs) that can work to about 1.2 THz, there is indeed only one proven solution: frequency multiplier chains from the microwave region to the terahertz [1], [11]. With current terahertz frequency multipliers, power is measured in microwatts rather than milliwatts. The current state-of-the-art at room temperature is 3 μW at 1.9 THz [12], 15–20 μW at 1.5–1.6 THz [13], [14], and 100 μW at 1.2 THz [15]. As predicted in [16], these powers improve dramatically upon cooling: the same sources produce, respectively, 30, 100, and 200 μW at 120 K.

Despite relatively low output power levels, frequency-multiplied sources have some decisive advantages that make them the technology of choice for building the local oscillators of heterodyne receivers: firstly, they are inherently phase lockable and frequency agile, secondly, they work at room temperature, or at moderate cryogenic temperatures for enhanced performance; thirdly, multiplier sources are robust enough, compact enough, and use a sufficiently low level of dc power to claim several years of heritage in the selective world of space technologies. From AURA [17] to the Herschel Space Observatory [18], frequency multipliers have demonstrated their real-world operability and are proposed for even more challenging missions to the outer planets [19].

The prospect of having a milliwatt-level broadband terahertz frequency-multiplied source would have seemed far fetched just a few years ago. This work will present a 0.9-THz frequency tripler that delivers more than 1 mW at room temperature when pumped with a fully solid-state source. This level of power has already enabled the demonstration of an 840–900-GHz fundamental balanced Schottky receiver that exhibits state-of-the-art noise and conversion loss [20]. It can also enhance terahertz imaging applications by driving frequency multipliers to even higher frequencies [21]–[23], such as the 2.5–2.7-THz band.

Considering these new results, as well as recent advances in thermal management of frequency multipliers [24], the continuous progress of power amplifiers around or above 0.1 THz [25], and the prospect of high-breakdown-voltage GaN Schottky diodes for submillimeter-wave multipliers [26], [27], it is clear that electronic coherent sources have the potential to deliver

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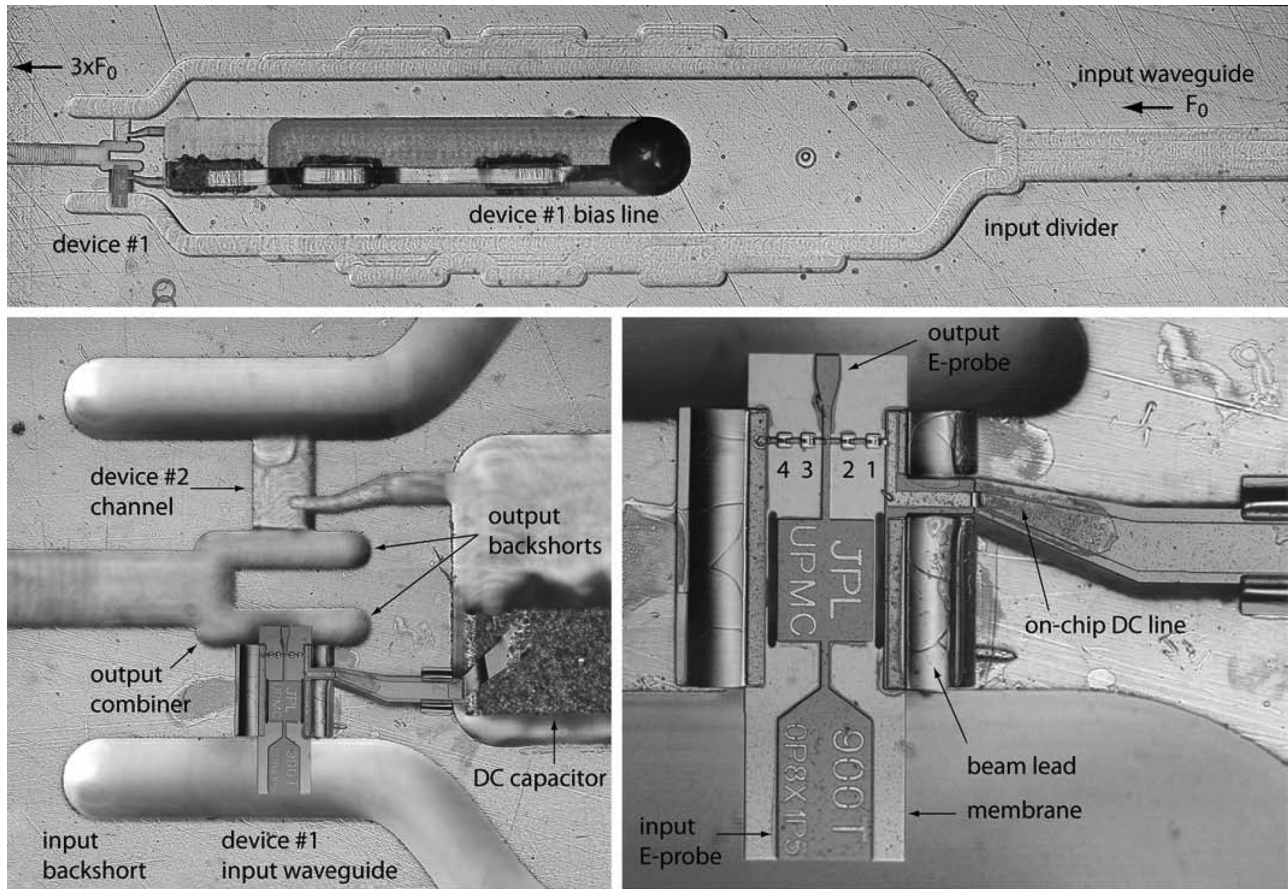


Fig. 1. Photograph of the bottom half of the power-combined 900-GHz frequency tripler showing device #1 (top view). Close-up view of the output combiner, device #1 and the dc capacitor (bottom left view.) Close-up view of device #1 with labels for diodes #1–#4 (bottom right view.). The tripler chip is approximately 300- μm long and 100- μm wide.

milliwatts of tunable single-mode power well into the terahertz range.

The present approach, however, is based on the concept of power combining demonstrated recently at 300 GHz [28] and on the technological heritage of the past few years in planar GaAs Schottky diode multipliers. The source that will be presented is based on a power amplifier module at W -band that pumps two frequency triplers that are cascaded. The first stage tripler utilizes four devices, while the second tripler is based on two devices and will be the focus of this paper. This unprecedented approach enables compact broadband sources with milliwatts of output power near 1 THz.

II. DESIGN AND SIMULATIONS

A. Design

The power-combined 900-GHz tripler is based on two identical chips that are power combined in-phase in a single waveguide block using a Y-junction divider at the input waveguide and a Y-junction combiner at the output waveguide. The chip was first used for a single device version of the 900-GHz tripler before being employed in the current design.

Fig. 1 shows an overall photograph of the tripler including the input matching circuit and two different close-ups of the device area. The tripler uses a symmetrical split-block waveguide design with one device mounted in each half block. The input

waveguide is split in two by a compact Y-junction to evenly feed the devices that are mounted in a channel that runs between their respective input and output waveguides. The two reduced-height output waveguides are combined by a Y-junction that is seen by each branch of the circuit as a simple waveguide step.

Each device features four Schottky varactor diodes monolithically integrated on a 3- μm thin GaAs membrane in a balanced configuration and biased in series. Each anode has an intrinsic zero bias capacitance of about 4 fF. An E -plane probe located in the input waveguide couples the signal at the input frequency to a suspended microstrip line. This line has two sections of high impedance (about 130 Ω at 900 GHz) and one section of medium-low impedance (about 50 Ω at 900 GHz) to prevent the third harmonic from leaking into the input. The third harmonic produced by the diodes is coupled to a short section of a high-impedance line and then to the output waveguide by a second E -plane probe.

As for the 300-GHz tripler, the dimensions of both the channel and circuit are chosen to cut off the TE mode at two-third of the highest frequency of the desired band to insure that the second harmonic of the input signal is trapped in a virtual loop, i.e., the diode loop. This condition is necessary, though not sufficient, to balance the circuit [29].

The balancing has to be precise if the multiplier is to achieve high conversion efficiency from the fundamental frequency to

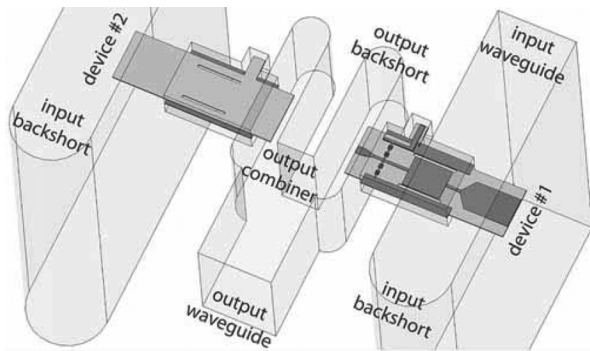


Fig. 2. 3-D view of the inner part of the 900-GHz in-phase power-combined frequency tripler as modeled with Ansys HFSS for simulations at the output frequency. The two chips, part of the input waveguides, the output waveguides, and the output combiner are represented.

the third harmonic [29]. This is helped by the use of fewer pairs of diodes with small mesas. However, high-power frequency multipliers require the use of as many diodes as possible [30], [31]. The multiplier presented in this paper was designed for 40 mW of input power and can handle up to 60 mW.

To increase the spectral purity of the 900-GHz frequency multiplier chain, the dimensions of the output waveguide has been chosen to cut off any second harmonic leakage that could result from circuit unbalance. In addition, the balanced geometry of the circuits ensures that power at the fourth harmonic of the input is strongly suppressed. The closest harmonic that can leak is the fifth at 1500 GHz, but, given the capacitance of the diodes, no significant power is expected at this frequency. As seen later in this paper, experimental results show that the chain achieves an excellent spectral purity at all the frequencies of the design band.

As mentioned in [29], to extend the bandwidth, the input matching network includes several sections of waveguide of different heights and lengths.

B. Simulations

Predicted performance of the multiplier were obtained using the same method as in [28] and [29]. Our diode model was adjusted for the actual anode size ($1.2 \mu\text{m}^2$) and for the epilayer doping ($5 \times 10^{17} \text{cm}^{-3}$). The multiplier structure was decomposed in several blocks that were analyzed separately with a 3-D electromagnetic field solver (Ansys High Frequency Structure Simulator (HFSS)¹). Fig. 2 shows one of the sub-circuits used for simulating the linear response of the multiplier at the output frequency. The different blocks were then assembled in a circuit simulator (Agilent Advanced Design System (ADS)²) to perform harmonic-balance simulations of the whole circuit and to determine a number of parameters related to the performance of the multiplier.

Among them, the balancing of the diode at the input frequency was investigated in detail to avoid the risk of overdriving a diode. The top graph of Fig. 3 shows the input coupling efficiency of each diode of one of the chips in the 775–950-GHz band for a flat input power of 45 mW and a reverse bias voltage

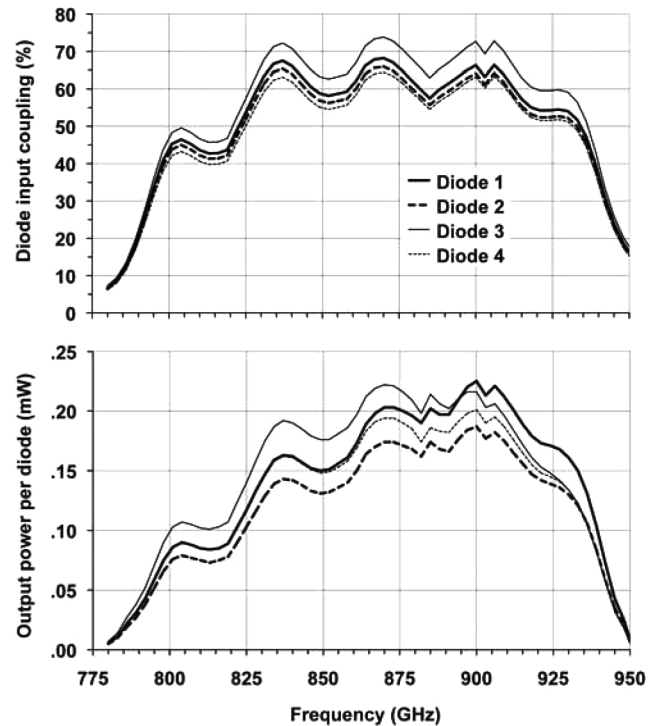


Fig. 3. Simulated response of the 900-GHz in-phase power-combined frequency tripler when pumped with 45 mW of input power and a fixed bias of -2 V (for four diodes in series per chip): the top graph shows the input coupling efficiency of the four diodes of one of the chips, and the bottom graph shows the power produced by each diode of the same chip.

of 2 V. All simulations include waveguide losses and assume that the multiplier circuit is symmetrical; therefore, the second chip behaves exactly the same (no study on the effects of mechanical and electrical asymmetries between the chips has been pursued for this study). According to these simulations, the balancing at the input frequency is better than 2% for diodes #1, #2, and #4 with only diode #3 receiving less than 10% more power than the other three (see Fig. 1 to locate each diode on the chip).

The bottom graph of Fig. 3 shows the power produced by the same diodes at the output frequency. The balancing is significantly degraded, but remains within $\pm 15\%$ at the center of the band. It is notable that diode #4, which receives less input power than diode #2, does actually produce more power at the output frequency. No detailed investigation have been pursued to explain this, however, other simulations on this particular circuit, or simulations performed on similar circuits at other frequencies, suggest that such reversal in the input and output balance is related to the proximity of the diodes to the channel opening into the output waveguide. Depending on the position of the output backshort, this reversal can be observed or not, showing that the output backshort has an asymmetrical impact on the diodes (pushing the diodes further back inside the channel does reduce this asymmetrical impact, but at the expense of the multiplier performance).

Fig. 4 shows the output power and the output coupling efficiency, which is defined as the ratio of the output power by the sum of the power produced individually by the diodes. All simulations do include the effects of the waveguide losses and are performed with a flat 45 mW of input power and a bias voltage of -2 V. From 775 to 865 GHz the output power rises from almost zero to 1.3 mW and then stays flat up to about 905 GHz

¹HFSS, Ansys Inc., Pittsburgh, PA.

²ADS, Agilent Technologies, Palo Alto, CA.

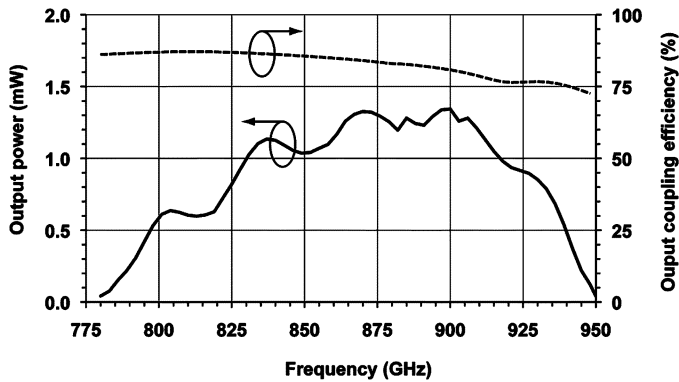


Fig. 4. Simulated response of the 900-GHz in-phase power-combined frequency tripler when pumped with 45 mW of input power and a fixed bias of -2 V (for four diodes in series per chip): the top curve (dashed line) shows the output coupling efficiency and the bottom curve (solid line) shows the output power.

before declining to almost zero at 950 GHz. The 3-dB bandwidth extends from approximately 820 to 930 GHz. The output power efficiency, however, declines slowly from 87% to 75% from 775 to 940 GHz, and then drops to 70% at 950 GHz. From Figs. 3 and 4, it clearly appears that the multiplier bandwidth is limited by the matching at the input frequency.

III. MEASUREMENTS

We assembled and tested several tripler blocks. Assembly was a bit more complex as for our dual-chip 300-GHz tripler, essentially due to bended shape of the dc line. The output power and the conversion efficiency of the 900-GHz power-combined frequency tripler were measured at room and cryogenic temperatures.

A. Driver Stage

The driver chain of the 900-GHz in-phase power-combined frequency tripler is constituted by a W -band synthesizer followed by a high power power-combined W -band amplifier module, and a power-combined 300-GHz frequency tripler based on [28]. The power delivered by the driver stage at 300 GHz was measured using a waveguide Erickson Instruments power meter [32] and a 1-in-long WR10–WR3 waveguide transition to match the multiplier output waveguide. When pumped with 330–500 mW, this tripler delivers 29–48 mW in the 276–321-GHz band (see top graph of Fig. 5). The maximum power that can be handled by this multiplier is based on thermal modeling of the chip.

B. Frequency Sweeps at 295 K—Comparison With Simulations

At room temperature, the output power of the 900-GHz tripler was measured using an Erickson Instruments power meter and a 1-in-long WR10–WR1 waveguide transition to match the multiplier output waveguide. As for the calibration of the input power, the measurements of the output power of the 900-GHz tripler were not corrected for waveguide transition losses. The 900-GHz tripler output power was measured in the 826–950-GHz band every 1.8 GHz. The two bias voltages of the 900-GHz tripler were optimized independently at each frequency. The biases range between -2.5 V to -1 V for four

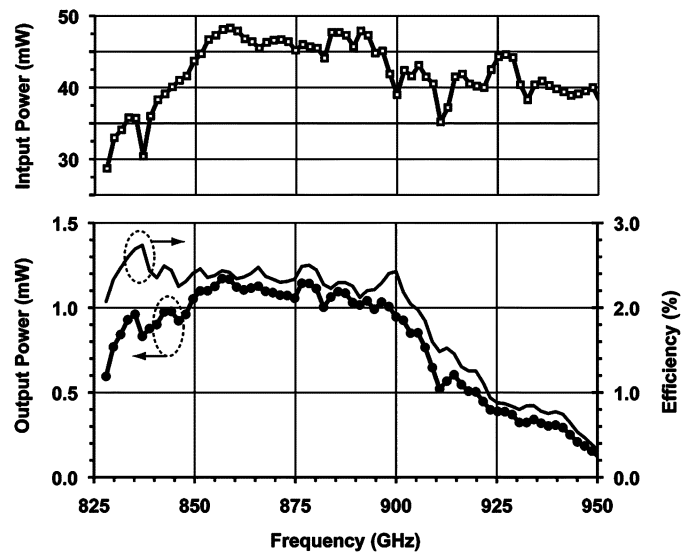


Fig. 5. Input power (top graph with square open markers), output power (bottom graph, bottom curve with round filled markers), and conversion efficiency (bottom graph, top curve with thin line and no markers) at 295 K of the in-phase power-combined 900-GHz frequency tripler measured with an Erickson Instrument power meter and a matched waveguide transition. The losses of the transition are not taken into account. The bias voltages were optimized at each frequency point and the structure in the measured plot can be due to interaction between the two triplers. The measurements were made using a power amplifier that delivers 330–500 mW from 92.0 to 93.0 GHz (828–837-GHz multiplier chain output frequency) and a fixed 500 mW from 93.0 to 105.5 GHz (837–950-GHz multiplier chain output frequency).

diodes in series at dc, and the rectified currents do not exceed 1.2 mA.

Conversion efficiencies were calculated by dividing the power levels recorded at the output of the 900-GHz chain by the power levels recorded at the output of the driver stage. As there is no isolator between the two stages, the actual value of the efficiency may differ due to a possible interaction between the two triplers.

Fig. 5 shows that the 900-GHz power-combined frequency tripler produces over 1 mW from 849.6 to 898.2 GHz at room temperature with a peak power of 1.2 mW at 857 GHz. The conversion efficiency is in the range of 2.1% to 2.5% in the same frequency range. Between 900–950 GHz, the tripler output power and efficiency decrease from 1 to 0.2 mW and from 2.4% to 0.3%, respectively.

Fig. 6 shows a comparison of the measured conversion efficiency with the predicted efficiency when taken into account the measured values of the 900-GHz tripler input power. Therefore, these simulations differ from those presented in Fig. 4 where a flat 45 mW of input power was assumed. Fig. 6 shows a good agreement between the measurements and the simulations, except at the high end of the band where the roll-offs have a different slope.

C. Frequency and Power Sweeps at 120 K

The chain was tested at cryogenic temperature in a different setup. The W -band power amplifier was replaced with a slightly different one and was left outside the cryostat, while the 900-GHz tripler and its driver were mounted inside. A corrugated horn directly attached to the output flange of the

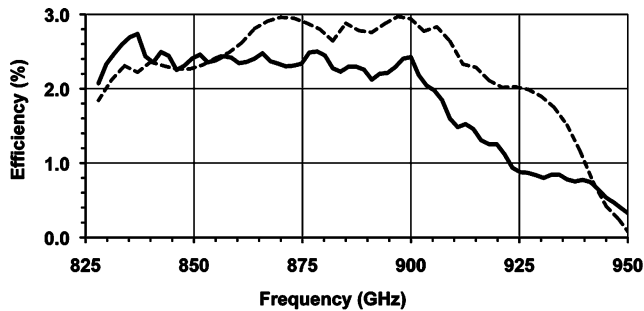


Fig. 6. Predicted (dashed line) and measured (solid line) tripler conversion efficiency of the in-phase power-combined 900-GHz frequency tripler. The measured values of the 900-GHz tripler available input power were used for the simulations.

900-GHz tripler and a mirror were used to focus the beam to the window of the Thomas Keating power meter. The modulation of the output beam was achieved by the W -band synthesizer at about 23 Hz to avoid the use of an optical chopper.

The cryostat window was made with a 25- μm -thick Mylar film that introduced limited RF losses, in the range of 9%–17%. These losses were measured at each frequency point and taken into account, contrary to the losses of the corrugated horn, which were not measured, and consequently, not taken into account.

The temperature was measured on top of the 900-GHz chain near the input flange of the 900-GHz tripler. As the cryostat uses an active cooling that can reach 15 K, heaters had to be used to maintain the temperature of the chain at 120 K within ± 2 K.

Fig. 7 shows a comparison of the frequency response of the 900-GHz multiplier chain when cooling from an ambient temperature of 295 to 120 K from 837 to 937 GHz with a frequency step of 4.5 GHz. The power at W -band does not change with the temperature and is limited to 500 mW since only the 900-GHz tripler and its driver stage are cooled. The improvement in performance depends strongly on the frequency. In the center of the band, between 835–900 GHz, the improvement varies between 20% at 846 GHz and 90% at 900 GHz. At 928 GHz, the improvement is about 100%. At an ambient temperature of 120 K, with a power at W -band limited at 500 mW, the output power peaks at 1.9 mW at 886.5 GHz, and at 1.8 mW at 900 GHz.

It is also noticeable that the power measured with the Thomas Keating power meter at room temperature in Fig. 7 matches the power measured with the Erickson Instruments power meter in Fig. 5 with a difference lower than +20%, or +0.75 dB, in the band where the W -band amplifiers deliver the same amount of power to the 900-GHz multiplier chain. Given the difference of setup and the fact that no power standard exists in this band, this discrepancy can be considered as very limited.

At 120-K ambient temperature, the power delivered by the W -band amplifier that drives the 900-GHz multiplier chain was swept from 200 to 550 mW. Fig. 8 shows the output power of the 900-GHz chain versus input power at W -band. A record output power of 2 mW was measured at 882 GHz for an input power of 550 mW. At this frequency, the output power increases almost linearly for input power ranging from 200 to 500 mW. Some saturation starts to occur at 500 mW of input power. At 900 GHz, the chain behaves almost the same as at 882 GHz, but starts to saturate at 450 mW.

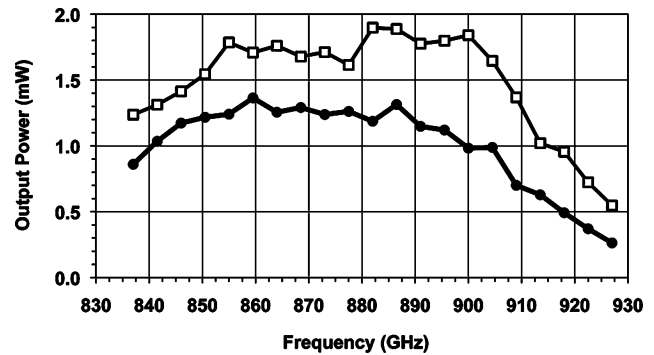


Fig. 7. Output power at 120 K (top curve with open markers) and at 295 K (bottom curve with filled markers) of the in-phase power-combined 900-GHz frequency tripler measured with a Thomas Keating power meter and a matched corrugated feed-horn. The measurements were not corrected for the losses of the horn. The bias voltages were optimized at each frequency. The measurements were made using a slightly different amplifier than for the measurements presented in Fig. 5. The amplifier delivers 390–500 mW from 93.0 to 94.5 GHz (837–850.5-GHz multiplier chain output frequency), a fixed 500 mW from 94.5 to 101.5 GHz (850–913.5-GHz multiplier chain output frequency) and 500–395 mW from 101.5 to 103.0 GHz (913.5–927-GHz multiplier chain output frequency).

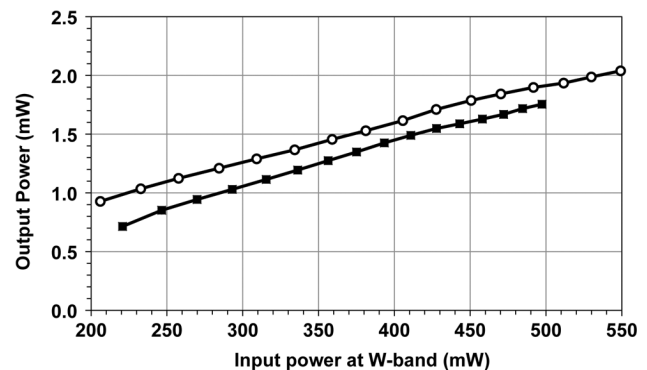


Fig. 8. Power sweep at an ambient temperature of 120 K of the 900-GHz frequency multiplier chain at 882.0 GHz (top curve with open markers) and at 900.0 GHz (bottom curve with filled markers).

D. Fourier Transform Spectrometer (FTS) Scans

The spectral purity of the 900-GHz frequency multiplier chain was checked from 0.15 to 2.1 THz using an FTS with 100-MHz resolution. Scans at different frequencies across the band have been performed. The scans were performed at room temperature. Fig. 9 shows the measured response at four frequencies covering the center of the band and its edges. The chain spectral purity is remarkably good with spurious or undesired harmonic below -27 dB with respect to the main signal, except at the high end of the band where the second harmonic of the 900-GHz tripler pump signal can be detected at a level of 10 dB below the third harmonic. Although the 100-MHz resolution of the FTS does not allow resolving low-frequency spurious signals around the main carrier, nor determine the level of phase noise, extensive tests of such multiplier chains have been done in the past and have shown that spurious signals and phase noise do not relate to the frequency multipliers themselves, but rather to the quality of the power supplies, to the fact that the power amplifiers are saturated or not, and to the phase noise of the synthesizer itself. Fig. 9 shows that a

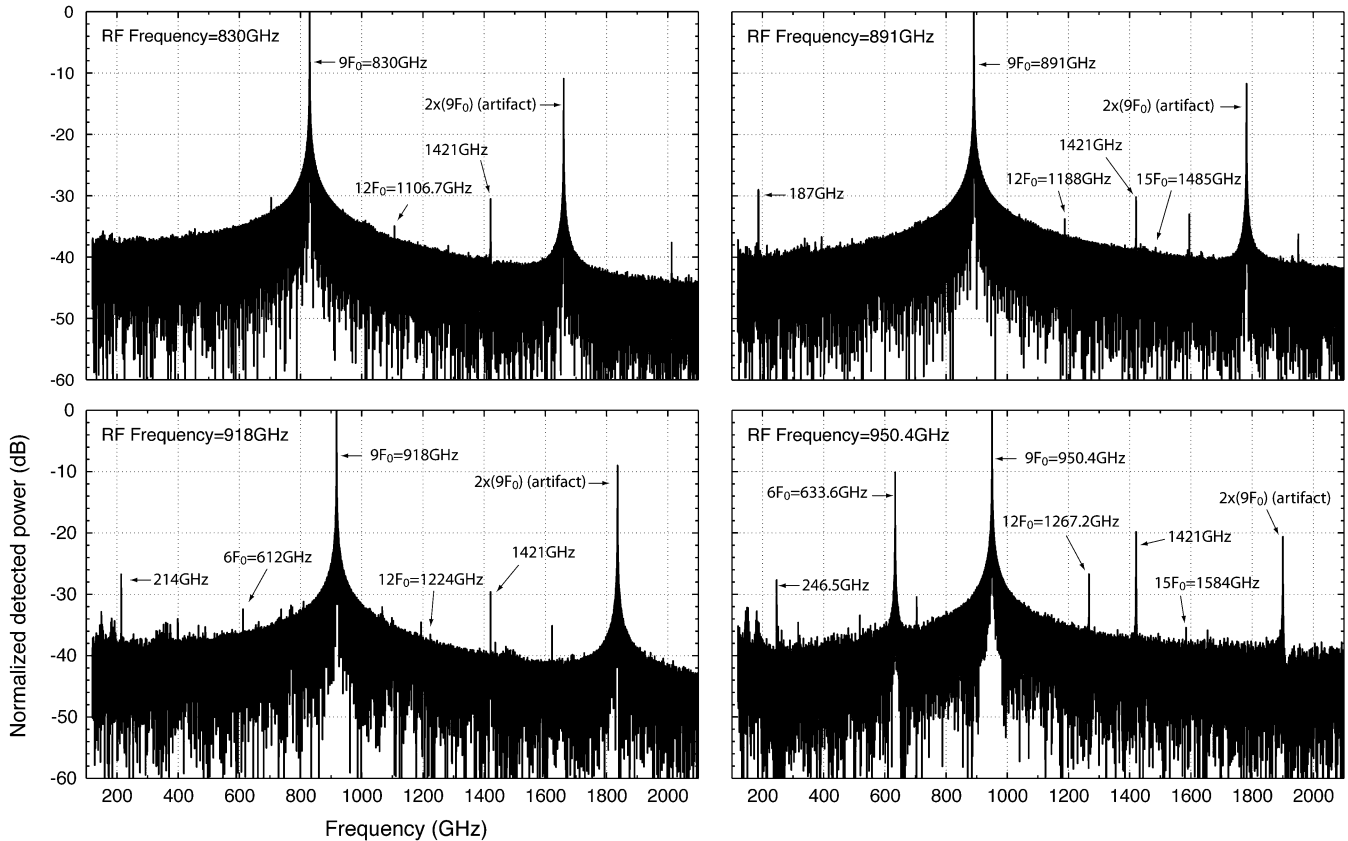


Fig. 9. FTS scans with 100-MHz resolution of the 900-GHz frequency multiplier chain at 830.0 GHz (top left), 891.0 GHz (top right), 918.0 GHz (bottom left), and 950.4 GHz (bottom right). For each scan, the graph is normalized to the peak power that corresponds to the ninth harmonic of the input frequency F_0 at W -band. It can be seen that the chain has an excellent spectral purity for the design band with spurious or undesired harmonic below -27 dB with respect to the main signal. At the edge of the band (950.4 GHz), the sixth harmonic of the last stage tripler starts to be significant with a recorded relative level of -10 dB with respect to the main signal. The cutoff frequency of the second stage is 633 GHz, and thus, at the band edge, this signal starts to leak through the multiplier. Note that the FTS graphs show a strong signal at exactly twice the frequency of the main signal: it is actually an artifact (aliasing) due to the FTS itself. The twelfth harmonic is detected, but is very weak, as expected. The fifteenth harmonic is detected only at 891 and 950.4 GHz and is even weaker than the twelfth harmonic. A line at 1421 GHz is detected in all the scans and cannot be explained. Lines at 187, 214, and 245.5 GHz are detected for, respectively, the RF frequencies of 891, 918, and 950.4 GHz. These lines are at frequencies well below the cutoff frequency of the 900-GHz tripler output waveguide and are, respectively, 11.3, 12.6, and 14.0 times the synthesizer frequency that generates the pump signal at W -band. The synthesizer frequency is one-sixth of F_0 or one fifty-fourth of the output frequency. Other signals with unexplained origins are also detected in some scans.

cascade of two balance triplers designed to suppress unwanted harmonics can actually achieve that goal at about 1 THz.

IV. CONCLUSION

A broadband solid-state source with more than 1 mW of output power across the 840–900-GHz band has been demonstrated. When cooled to 120 K, the output power increases to a peak of 2 mW. These power levels were made possible by the use of in-phase power combining of frequency multiplier chips. This source will be used to drive a third frequency tripler currently under development for use as the local oscillator of a 2.5–2.7-THz heterodyne receiver. While no systematic reliability study has been done on this source, it should be pointed out that the chips used are based on a space-qualified technology that has been designed for reliability.

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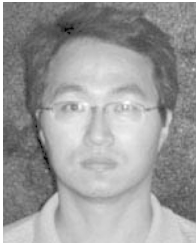
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