200 AND 400 GHZ SCHOTTKY DIODE MULTIPLIERS FABRICATED WITH INTEGRATED AIR-DIELECTRIC "SUBSTRATELESS" CIRCUITRY

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Abstract

A novel semiconductor fabrication process has been developed at the Jet Propulsion Laboratory for realizing millimeter and submillimeter-wave monolithic integrated circuits. The process enables integration of the active devices, Schottky diodes, with planar metallic transmission lines. To reduce the RF losses in the passive circuitry, the semiconductor substrate under the transmission lines is etched away, leaving the metal suspended in air and held only by its edges on a semiconductor frame. The frame also allows the circuit to be handled and mounted easily, and makes the whole structure more robust. Moreover, this technology allows for the diodes to be positioned precisely with respect to the circuitry and can be scaled for higher frequency applications. Metallic beam-leads are used extensively on the structure to provide mechanical 'handles' as well as current paths for both DC grounding and diode biasing. To demonstrate the utility of this technology, broadband balanced planar doublers based on the concepts in [1] have been designed in the 200 and 400 GHz range. Extensive simulations were performed to optimize the diodes and design the circuits around our existing device fabrication process. The 368-424 GHz circuits were measured and achieve 15% peak efficiency at 369 GHz. The 3-db bandwidth of the fix-tuned doubler is around 9%. The maximum output power measured is around 6 mW and drops down to 1mW at 424 GHz. This represents the highest frequency waveguide based planar doubler to date known to the authors.

1 Introduction.

High-resolution spectroscopy missions in the context of astrophysical, Earth and planetary observations are increasingly in demand [2]. The objective of the Far-Infrared and Submillimeter Space Telescope (FIRST) mission is to study the formation and evolution of galaxies in the early universe, stellar formation, and the interstellar medium [3,4]. The heterodyne instrument for FIRST (HIFI) is intended for high resolution observations of molecular lines in bands stretching from 500 to 2700 GHz, many of which can only be made from space because of atmospheric absorption. For maximum sensitivity these heterodyne instruments use either superconducting insulating superconducting (SIS) or hot electron bolometer (HEB) mixers.

The mixers require local oscillator (LO) power in the range of tens of microwatts for the SIS mixers and hundreds of nanowatts for the HEBs. The goal of the technology development program for the LOs at JPL is to enable construction of solid-state sources into the THz range which achieve the required output power over bandwidths of ten percent or more. Using current technology this requires a cascade of doublers and triplers. For example, Figure 1 depicts the FIRST band 5 receiver LO system along with the bandwidth and power requirements [5]. Complex missions such as FIRST require up to 100 or more multiplier units. Due to the large number of required multiplier components, a modular design which reduces cost and simplifies assembly is essential. Additionally, the multipliers must be rugged enough to withstand the temperature, shock and vibration extremes associated with space missions, and must go through a rigorous space qualification process to demonstrate compliance with mission demands.

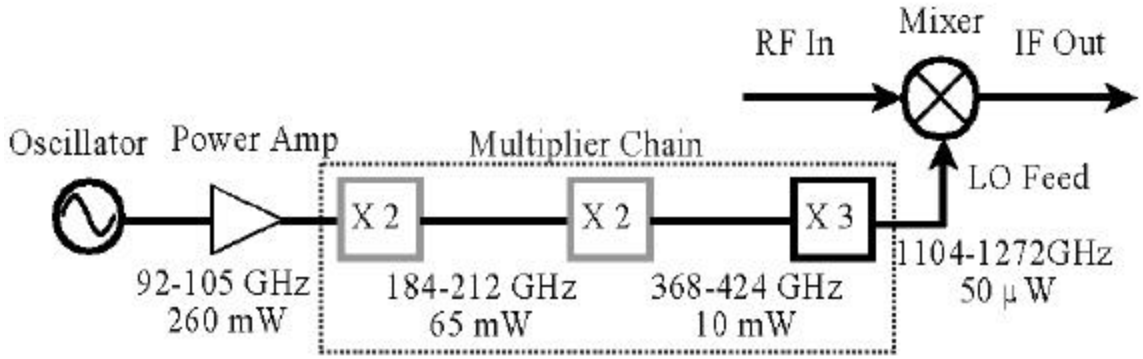

Figure 1. FIRST LO band 5 receiver. Bandwidth is 14 %.

There has been considerable development and improvement of planar Schottky diode multipliers in the last few years. However, the required power and bandwidth performance specifications for the FIRST LO sources remain challenging. The highest frequency multiplier circuit reported to date is a tripler to 1395 GHz, which produces about 17 **m**W of power with a input power of 7 mW from a carcinotron source [6]. The diode used in this multiplier is a whisker contacted Schottky and the circuit is a traditional crossed waveguide block. The highest frequency all solid state multiplier chains reported to date are around 1000 GHz. These used InP Gunn diode oscillators at 111.2 GHz followed by two whisker-contacted triplers in series and obtained output powers of 60-120 ?W [7].

At lower frequencies, balanced planar Schottky diode multipliers have been reported in the 350 GHz range with about 5 mW of output power [8]. Balanced doublers incorporate symmetrical pairs of diodes to simplify the circuit design. It is now possible to design and build very high power multipliers in the 150-320 GHz range that can be used to drive follow on stages. 80 mW at 140 GHz, 76 mW at 180 GHz, and 15 mW at 270 GHz have already been demonstrated and a number of variations of the balanced doubler concept [9] have yielded very impressive results [8?11]. In order to realize multiplier chains to 2500 GHz it is essential that the lower frequency stages be capable of handling large

input powers around 250 mW.

The multipliers each consist of two components – the nonlinear solid state device (the Schottky diode) and the surrounding input, output and impedance matching circuitry. To meet the challenges of FIRST successfully it is important to refine and advance both of these critical elements further. As the frequency increases and all relevant dimensions shrink, it often becomes difficult to separate the device from the circuit. This makes it important to optimize processing in combination with the circuit realization, assembly, and testing procedure.

Referring to Figure 1, the work described in this paper is on the two lower frequency doublers shown in gray. The final tripler is currently being processed using a somewhat different technology, and is described in a companion paper [12].

2 "Substrateless" technology.

Submillimeter-wave multiplier technology is undergoing a revolution in implementation and realizable performance, for two main reasons. First, the incorporation of planar GaAs diode MMIC topologies into high frequency circuits has progressed tremendously. This progress stems from improvements in the accuracy and reproducibility of the most dimensionally critical elements due to the use of e-beam lithography and the blending of traditional metal machining with semiconductor micromachining. Second, the availability of high performance CAD tools and models now permits much greater accuracy in the analysis and optimization of circuit performance.

The implementation of GaAs discrete diode chips is limited at very high frequencies for several reasons. In the most successful lower frequency balanced doubler designs [8?11], a small planar diode chip is mounted into a metallic waveguide block by means of solder or silver epoxy. DC bias and RF output coupling is implemented by means of a bond wire, a precision-machined coax structure, or a quartz circuit between the block and the chip [8,9]. A different approach has the diode chip soldered directly to a quartz-based filter which is inserted into the waveguide block with wire bonds used to connect the quartz circuit to the block [10,11,13]. In spite of the success of these designs, as the operating frequency increases, these mounting techniques become excessively difficult. For instance, the constraints of reduced waveguide size, increasing substrate loss and higher order mode suppression dictate the use of very thin substrates when at these frequencies, and the circuits must be very precisely aligned with the waveguide structure.

In order to circumvent these limitations we have proposed and demonstrated technology that can work well into the THz range. This technology relies on standard processing techniques such as stepper lithography and reactive ion etching to fabricate the diode structures on the front side of the wafer. After front side processing is completed a backside procedure is used to remove all of the GaAs under the matching circuit. Only a GaAs frame is left where necessary to support the matching structure. The Schottky

diodes are formed on one edge of this frame. The resulting "substrateless" structure thus has an all metallic matching circuit with no underlying dielectric with the active devices incorporated monolithically. The structure is physically much larger than previous diode chips thus allowing easier handling and mounting. Moreover, beam leads placed on the structure improve heat transfer and simplify the assembly procedure when mounting in the waveguide block.

3 Design methodology.

The multipliers are designed using a three-step process. The first uses a non-linear circuit simulator and a diode model implementation developed at JPL. This model is used with the harmonic balance based simulator to optimize the dimensions, doping profile, and number of diodes to be used in the circuit. This process yields the diode junction characteristics and embedding impedances which give the best performance.
Secondly, the multiplier input and output matching circuits are then designed using an electromagnetic (EM) finite-element based simulator. The numerical output of the EM simulator comprises scattering parameter matrices referenced to the diode and waveguide ports. These are then entered into a linear simulator along with the embedding impedances from the non-linear simulator to analyze the impedance matching effectiveness of the waveguide input and output circuits. The parasitics associated with the diode (mesa, air bridges) are included here as part of the passive circuit. To simplify and speed up the process, the passive circuitry is divided up into small elements at electromagnetically appropriate points, giving several S-parameter matrices. Ports are attached to probes on each anode so that the individual embedding impedances for each diode can be calculated directly. The diodes are then embedded into the resulting cascaded S-parameter matrix blocks to determine the total efficiency and power performance of the multiplier. If these are unsatisfactory compared to the intrinsic performance of the diodes, the circuit design is iteratively modified to correct for parasitics found with the full 3-D simulation.

More details on the simulation methods used for calculating embedding impedances for the diodes and the passive structure were presented in References [9,14,15]. This method has shown to produce good results, and is the basis for much of the recent breakthrough in multiplier performance below 1 THz [8–11]. Very good agreement between the results of this analysis approach and measurements has been found at least up to 350 GHz.

The 200 and 400 GHz doublers are designed to operate with input powers of 200 mW and 40 mW respectively. In order to handle these power levels without compromising efficiency more than one pair of diodes must be utilized. The 200 GHz design uses an array of six and the 400 GHz design uses four.

The designs shown here have been based upon the assumption that it is desirable to position the diodes in the input waveguide with most of the output matching circuitry close to the devices; hence, the complicated structure between the waveguide probe and

the diodes shown in Figure 2. The input impedance matching is accomplished in the input waveguide using the full to reduced height waveguide step, the backshort position and the diode geometry. The line extending across the output waveguide is an E-field probe, terminated on the right with a lowpass filter for DC bias. The diodes are grounded to the waveguide block with the two beam leads shown on the left. The beam leads on the right extending from the top and bottom of the GaAs frame are included only to make handling and positioning of the circuit in the waveguide block easier. The filter is a lowpass type which, while large, is effective, straightforward to design and does not require any special processing or additional assembly steps. The beam leads at the right (coming off the bias filter metal) are bonded to a single-layer chip capacitor as a DC standoff. From there a bond ribbon is connected to the input DC bias connector.

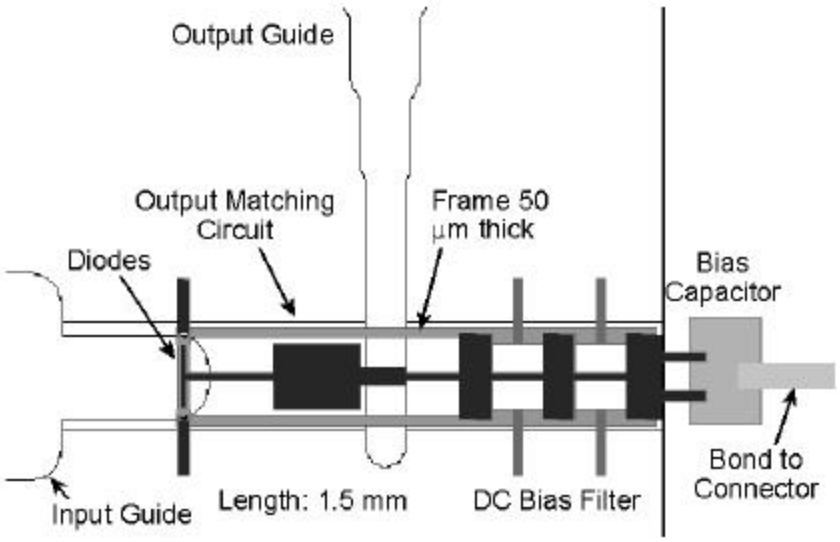

Figure 2. Schematic of 400 GHz doubler in block. 200 GHz version looks similar.

In the future the single layer capacitor used on the DC bias side of the output waveguide will be used without the low-pass filter, reducing the chip size by half. It is also possible to integrate a bypass capacitor directly on the monolithic chip. This makes the assembly alignment less dimensionally critical since a substantial fraction of the DC bypassing is achieved on chip. To further simplify the structure some of the output matching can be performed using stubs near the diode. A single short line will replace the matching structures between the diodes and output guide. The remainder of the output impedance matching is accomplished in the output waveguide.

4 Testing and results.

4.1 Test Set.

The test set is depicted in Figure 3. It consists of a W-band oscillator followed by a variable attenuator to compensate for oscillator output power variations. In the setup

shown the oscillator is a BWO, although a YIG oscillator followed by a sextupler has also been used. Following the attenuator is a W-band solid-state power amplifier module. This includes a driver whose output is coupled to a magic-T splitter feeding two PA modules. Their outputs are combined in another magic-T followed by a low-loss isolator before the 200 GHz doubler.

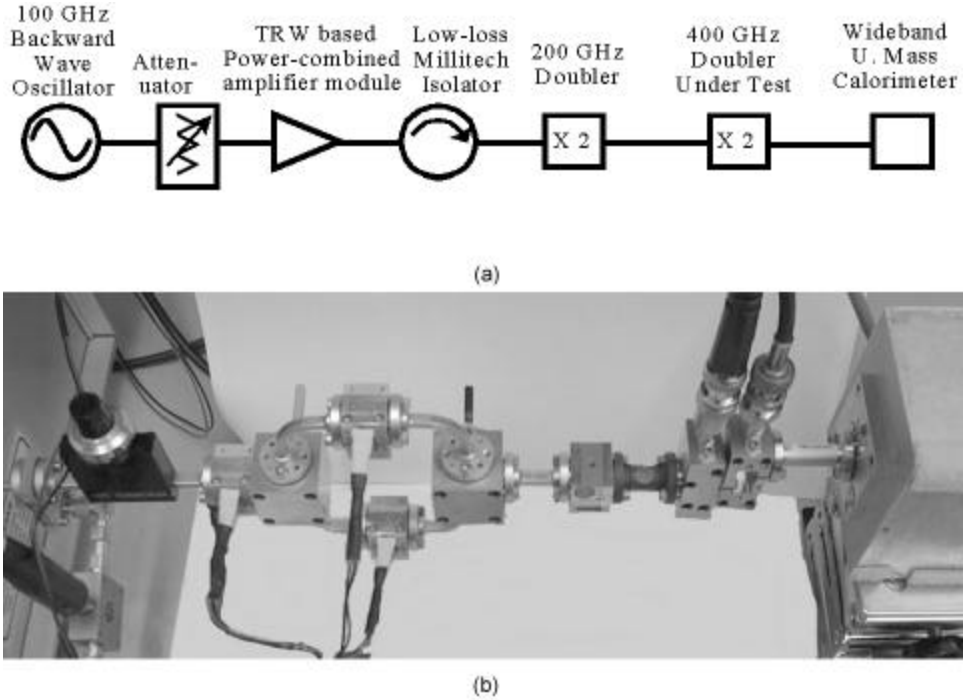

Figure 3. 400 GHz test set. (a) Block diagram. (b) Photo.

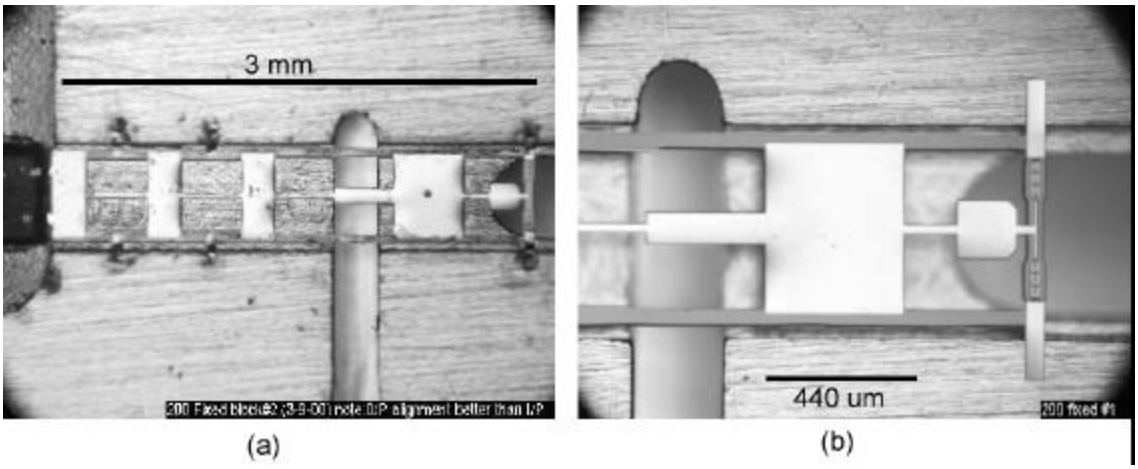

Figure 4. 200 GHz doubler in block. (a) Complete chip. (b) Closeup of diode region.

If this doubler is the device-under-test (DUT), a directional coupler is inserted between the isolator and the DUT with a W-band power meter in the coupled arm for monitoring

input power to the device. For testing the 400 GHz doubler the coupler is not used to maximize input power into the first doubler, which is directly connected to the second doubler as shown in the photo. In this case, a power sweep is made using the University of Massachusetts wideband calorimeter to determine the 200 GHz input power profile. In either case, during the DUT measurement the calorimeter is used to measure the output power. For the 400 GHz measurement a pass-through harmonic multiplier is inserted between the BWO and the attenuator to precisely measure the input frequency.

4.2 Assembly.

After completion of fabrication several 200 and 400 GHz doublers were assembled into waveguide blocks. For assembly the single-layer DC bias chip capacitor is first mounted into the empty block with epoxy. The SMA bias connector is then assembled into the block and a bond ribbon is added to between the connector and the bias capacitor. At this point the devices are simply placed into the channel of the block as shown in Figures 4 and 5. The grounding beam leads are bonded to the block surface with a bonding wedge, and the bias beam leads are similarly bonded to the capacitor top surface. Finally the block halves are assembled together.

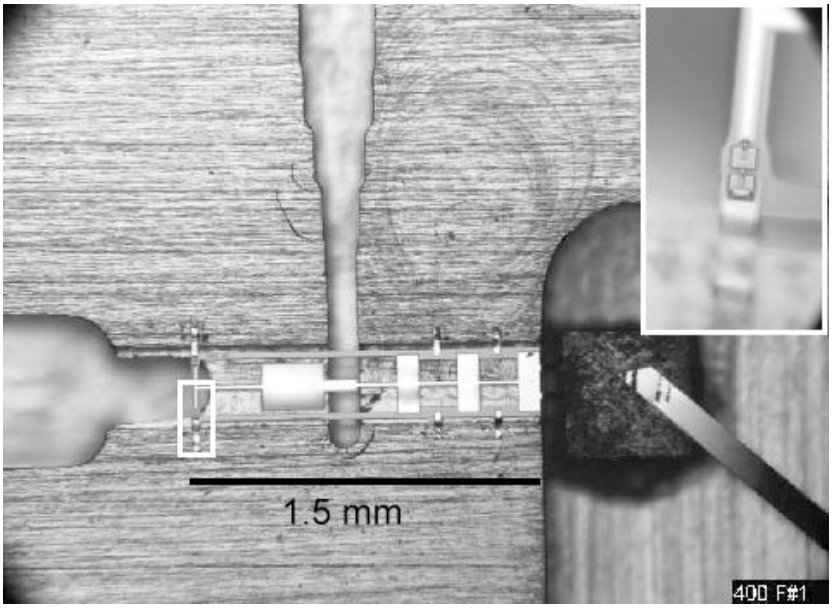

Figure 5. 400 GHz doubler in block. Inset shows closeup of diodes on frame.

4.3 Results.

The first doublers to be mounted and measured were the 200 GHz type. They showed an efficiency of 8 % over a narrow bandwidth, which is much less performance than designed. After further analysis it was found that there were several problems with the design. First, due to a machining error, the blocks that were delivered did not conform to the specified tolerances. Also, a design error made the circuit very susceptible to

positioning of the circuit in the block, as well as to variations in the machining of the block. These difficulties have been fixed in the next design iteration.

The performance of one of the 400 GHz doubler measured is portrayed in Figure 6. The efficiency varies between 10 and 15 % over the lower half of the band, with output power of 4 to 6 mW. This is the highest power and efficiency we know of reported to date over a comparable bandwidth for a varactor doubler.

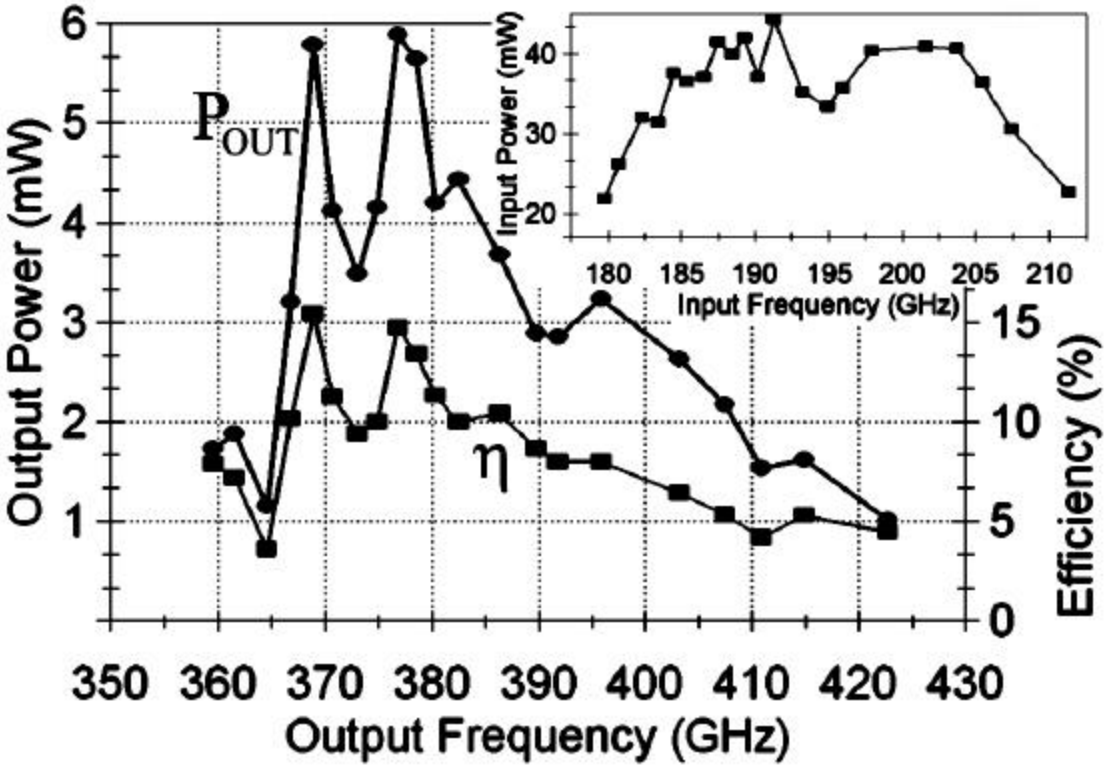

Figure 6. Measured efficiency, output power and input power of 400 GHz doubler.

5 Conclusions.

State-of-the-art multiplier performance using a new technology has been demonstrated. This technology is based on suspension of the passive circuitry across an etched semiconductor frame on which the active diodes are fabricated. This "substrateless" technique represents a new stage enabling the fabrication and performance of planar multipliers in the sub-millimeter and terahertz frequency range. A maximum power of 6 mW with a 3db bandwidth of 34 GHz has been demonstrated at 378 GHz. Work is continuing to improve the performance of the current designs along with an effort towards scaling this technology for the 700 to 1000 GHz range.

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