

HARMONIC BALANCE OPTIMIZATION OF TERAHERTZ SCHOTTKY DIODE MULTIPLIERS USING AN ADVANCED DEVICE MODEL

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Abstract — Substantial progress has been made recently in the advancement of solid state terahertz sources using chains of Schottky diode frequency multipliers. The multiplier diodes are often simulated using a simple Schottky junction model plus a series resistance, R_S , because of the model's simplicity and ease of use in commercial harmonic balance simulators. The DC series resistance value is useable for R_S at low frequencies, but at high frequencies the R_S must be increased to match the measured RF performance. The junction properties are determined from forward I-V measurement. We have developed a harmonic balance simulator and corresponding diode model that incorporates many other factors participating in the diode behavior. These include time-dependent velocity saturation, carrier inertia and shunt capacitance in the undepleted active layer, tunneling through the Schottky barrier and heating of the junction at high powers. The model is calibrated using ensemble Monte Carlo calculations of material parameters, but otherwise no parameters are fitted other than to DC I-V measurements. The program can be used to optimize the doping concentration and diode dimensions for any multiplier, based on its frequency, input power and operation temperature. Optimizations are demonstrated for 200, 400 and 800 GHz doublers, and comparison between calculation and measurement will be shown. The match between them will be seen to be quite close. Further, the measurements include new, low-temperature measurements of an 800 GHz chain yielding a high 2 mW peak output power.

I. INTRODUCTION

Currently there is a demand for wide-bandwidth frequency multiplier chains [1-3] with outputs above 1 Terahertz for use in submillimeter wave heterodyne receivers. These space-borne radiometers are primarily intended for astrophysical observation. The Jet Propulsion Laboratory has developed and implemented novel technologies to produce robust, reliable and repeatable planar Schottky diode multipliers for these applications

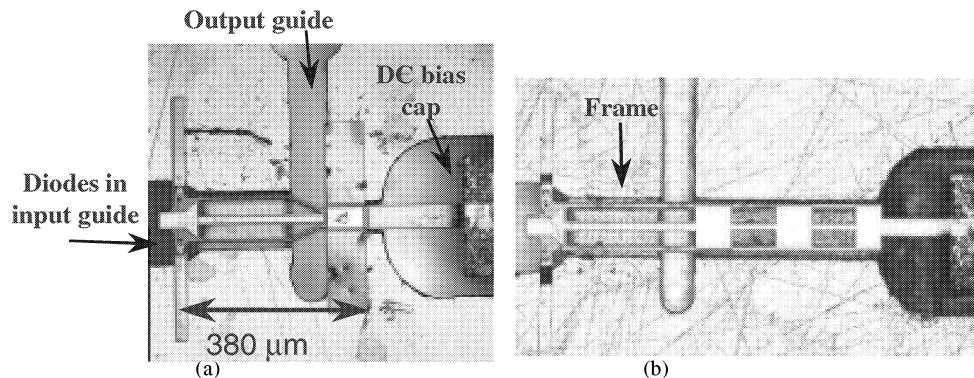


Figure 1. 800 GHz doublers mounted in block, both to the same scale. (a) is a version with on-chip bias capacitor, (b) uses a high-low transmission line filter for DC bias bypass.

[4]. In order to produce useable power at the final output frequency, the first stages in the chains are being pumped with high power levels of 200 mW or more at W-band [5]. Further, space missions such as the Herschel Space Observatory will be operated at low temperature, both for thermal margin and for improved multiplier performance [6]. There is a continuing effort at JPL to improve the modeling of the diodes, including

temperature, high frequency and high power effects. This paper will focus on a few recent additions to the diode modeling, as well as the results of optimization of diode characteristics for specific frequency/power/temperature combinations, and a comparison of multiplier simulations and measurements.

II. DESIGN AND ANALYSIS

The doublers consist of two components – nonlinear solid-state devices and surrounding passive circuitry. The devices are arrays of two to six Schottky diodes in a balanced configuration [7,8]. These are analyzed using a specially designed harmonic balance simulator. The surrounding passive input, output and impedance matching circuitry are analyzed using the HFSS finite element electromagnetic simulator. The circuit design process has been discussed previously [5,9-11], as has the fabrication [12]. An example of two versions of an 800 GHz doubler appears in Figure 1.

The harmonic balance simulator uses a modification of the reflection algorithm [13,14]. This method can incorporate an arbitrary set of differential equations in the diode model. Additionally, since the solution of the harmonic balance equations is an iterative relaxation process [15], during the course of the convergence such external variables as the bias voltage and the material properties can be varied in a controlled way. This allows the normal difficulty the method has of requiring an artificial DC embedding resistance [16] to be circumvented by adjusting the fictitious bias voltage so that the real bias will be the correct value. Additionally, the change in material properties with temperature can be incorporated via a thermal model to investigate the effect of heating in the high power multipliers.

The thermal model itself, described in an earlier paper [17], is a simple one-dimensional thermal resistance model that takes into account heat flow through the GaAs frame and the gold metalization. The results are in the form of a profile of the temperature of the anodes versus the dissipated power and the block temperature. The data from the calculation can be fit to a version of the thermal resistance model that is quadratic in power:

$$T_{ANODE} = T_{BLOCK} + R_{T1}P_{DISS} (1 + R_{T2}P_{DISS}) \quad (1)$$

where R_{T1} is the low-power thermal resistance, around 2.05 K/mW and R_{T2} is the correction, around 0.012 mW^{-1} .

This equation can then be incorporated into the material properties of the diode model, and its effect included in the harmonic balance investigation of the multiplier's performance.

III. DIODE MODEL IMPROVEMENTS

Since the diode model will be included in the iterative harmonic balance simulator, it needs to be fast. Therefore, we are using a modified equivalent circuit model. Most of the elements of the model have been reported earlier [17–20], so only recent modifications to the model will be discussed. The junction capacitance model, $C(v)$ includes the effect of fringing [21] as well as a version of the flatband capacitance [22-24] modified for numerical stability. The undepleted epi model includes carrier inertia modeled as an inductance, L_i , and shunt displacement capacitance, C_d [18]. The spreading resistance, skin effect impedance and ohmic contact impedance occur in the highly doped n^+ region, and their models are as before [17,18,20]. They are affected by the mobility in the n^+ GaAs, however, and that has been changed as described below. Modifications to the model of the junction current, $i(v)$ will also be covered.

A. Buried $n+$ layer mobility. In an effort to track down all causes of reduced efficiency, the mobility of highly doped GaAs, especially as a function of temperature, was investigated. Several measurements were found [25-27], which indicated the mobility is

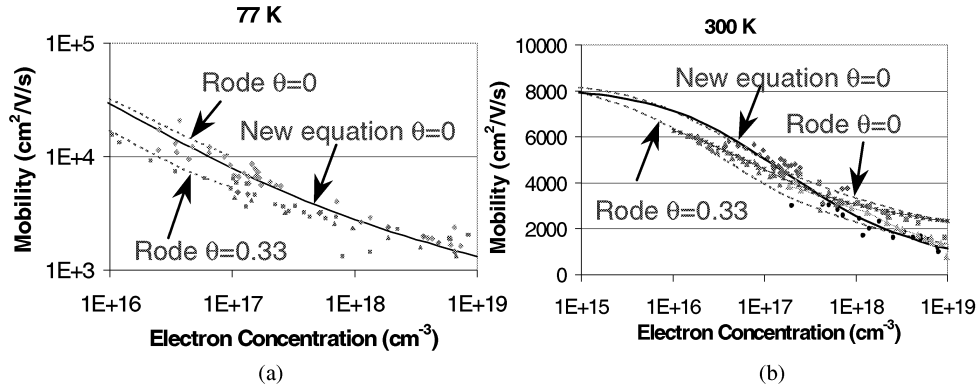


Fig. 2. GaAs Mobility at high doping concentrations. The broken lines are those of [40]. The solid line is the new formula. Dots are various measurements [25-27] (a) 77 K. (b) 300 K.

lower for doping concentrations above $5 \times 10^{17} \text{ cm}^{-3}$ than the values being used. The earlier equation [20] was based on the work of Rode and Knight [28,29]. A new equation was fitted, based on a combination of the measurements, Rode's work and others [30,31]. The results are indicated in Figure 2, which shows a combination of Rode's results, several measurements, and the new formula. The parameter θ is the compensation ratio of ionized acceptors to ionized donors, N_A/N_D^+ .

B. Junction current. Another source of reduced efficiency not previously included in the model is the reverse current increase due to avalanche multiplication. Previous calculations of the junction current incorporating barrier tunneling plus thermionic emission [20,32] and avalanche multiplication [20,33] matched measurements of actual diodes well [20].

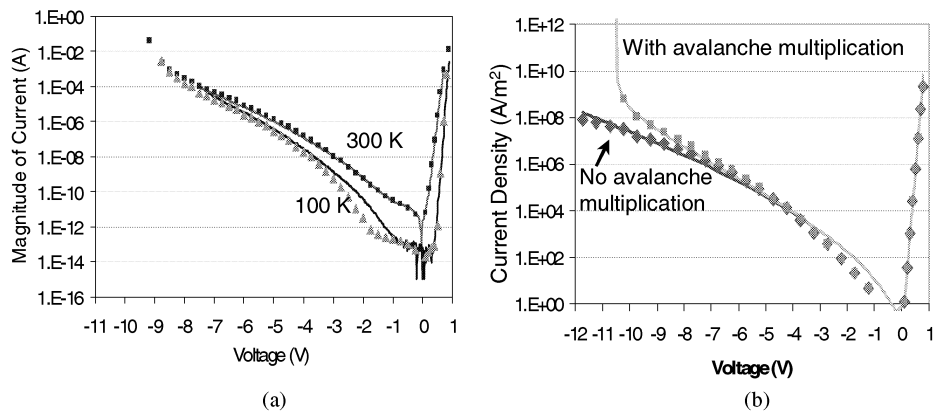


Fig. 3. Junction forward and reverse current magnitude. (a) Current measured for $45 \mu\text{m}^2$ anode, $3 \times 10^{17} \text{ cm}^{-3}$ doping (solid) compared to quantum transmission matrix calculation (markers). (b) Representative fit of transmission matrix calculation (markers) to fitted formula (solid), with and without avalanche multiplication.

A representative plot of the junction current is shown in Figure 3. Figure 3a, reproduced from [20], compares the junction current measured and calculated. These

apply to a diode having an anode area of $45 \mu\text{m}^2$ with an active layer doping of $3 \times 10^{17} \text{cm}^{-3}$, measured at 100 and 300 K. The junction current is calculated using the transmission matrix technique [32,34] and includes avalanche multiplication [33]. Since these calculations are too slow for the iterative solution required by the harmonic balance algorithm, the usual thermionic emission formula was modified to include reverse current

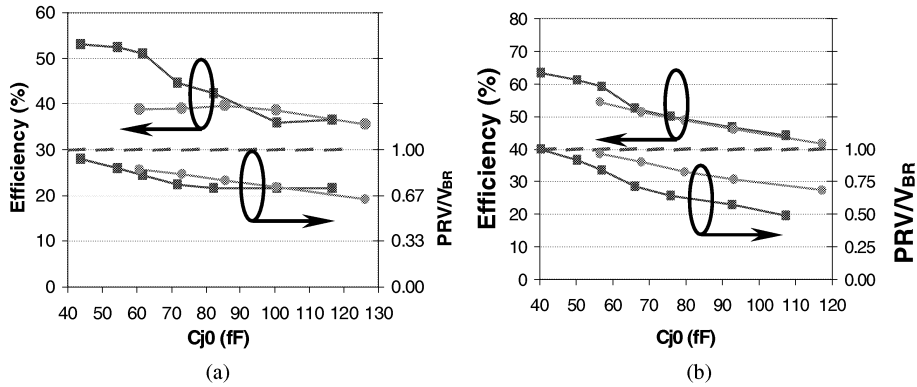


Fig. 4. Optimization of 200 GHz doubler. The input power is 33 mW per diode. Square markers reference $1 \times 10^{17} \text{cm}^{-3}$ doping, round markers $2 \times 10^{17} \text{cm}^{-3}$. (a) 300 K block temperature. (b) 120 K block temperature.

[17]. It now has been further modified to include the current increase due to avalanche multiplication.

Figure 3b compares the transmission matrix calculation with the values from the

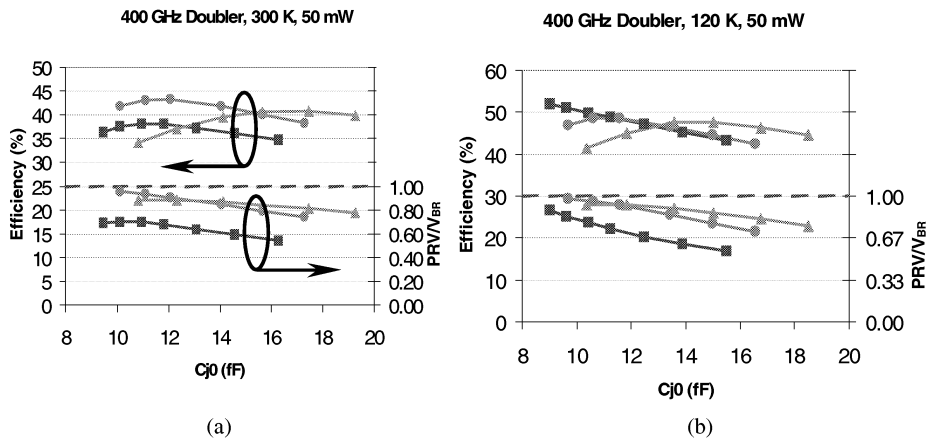


Fig. 5. Optimization of 400 GHz doubler. The input power is 7 mW per diode. Square markers reference $1 \times 10^{17} \text{cm}^{-3}$ doping, round markers $2 \times 10^{17} \text{cm}^{-3}$, triangle markers $3 \times 10^{17} \text{cm}^{-3}$. (a) 300 K block temperature. (b) 120 K block temperature.

modified thermionic emission equation used in the harmonic balance simulator.

IV. DOPING OPTIMIZATION

One of the primary reasons for performing this work is to determine optimum doping for multipliers at various frequencies, temperatures and pump powers. During the

fabrication process only one or two doping profiles can be included in a process run at a time. Since a range of multipliers is fabricated in each run, the dopings selected must represent a compromise among the various optimum dopings.

Figures 4 through 6 depict diode efficiencies calculated at block temperatures of 120 and 300 K for 200, 400 and 800 GHz doublers using diodes with several dopings. The results are plotted as a function of diode junction capacitance at zero bias, C_{j0} , since that is more characteristic of circuit tuning with frequency than diode area.

Shown on each plot is both the calculated efficiency and the ratio of the peak reverse voltage (PRV) during the pump cycle to the breakdown voltage. The limitations on the diode efficiency are 1) the diode series resistance; 2) junction current, which represents a circuit loss; 3) current saturation; and 4) the bias voltage and pump power must be limited in order to prevent diode damage. Reverse current is more destructive at a given power level than forward current as discussed in [36]. Therefore, prudence dictates that the multiplier design include a safety margin between PRV and breakdown voltage, V_{BR} . Work is continuing at JPL to find an appropriate margin, but at this point it seems that the PRV/V_{BR} ratio should be less than about 0.8.

The results indicated in Figures 4 through 6 can be compared to the analytical optimum doping formulas given in [37]. These equations incorporate the limitations to diode multiplier performance due to junction breakdown and current saturation, both of which are functions of doping and temperature. Further, they assume a particular profile of the diode waveform during the pump cycle that is consistent with the results we have found. Since the formulas don't take account of the series resistance, they can't determine the achievable efficiency.

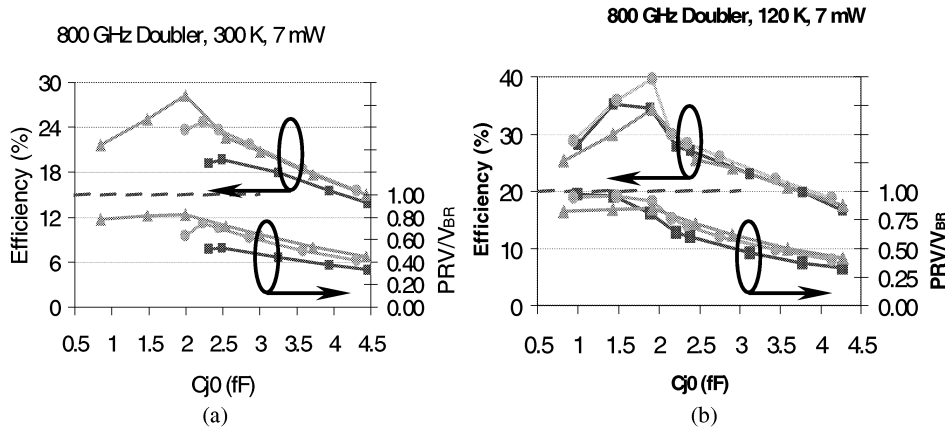


Fig. 6. Optimization of 800 GHz doubler. The input power is 3.5 mW per diode. Square markers reference $2 \times 10^{17} \text{ cm}^{-3}$ doping, round markers $3 \times 10^{17} \text{ cm}^{-3}$, triangle markers $4 \times 10^{17} \text{ cm}^{-3}$. (a) 300 K block temperature. (b) 120 K block temperature.

Assuming the active epi-layer is made just thick enough that the breakdown and depletion region punch-through occur at the same time, equations (1) and (2) of [37] can be combined with the standard expression for depletion width [38] to yield:

$$N_D(opt) = \frac{8f_{out}^2 \epsilon}{v_{pk}^2 q} [V_{bi} - PRV(N_D, T)] \quad (2)$$

where $N_D(opt)$ is the optimum doping, f_{out} is the multiplier output frequency, v_{pk} is the peak electron drift velocity, ϵ and q are the semiconductor permittivity and the electron charge respectively, and V_{bi} is the built-in voltage — about 0.8 V. Since the parameters are doping dependent, equation (2) must be solved iteratively. However, convergence is fast.

To determine a value for v_{pk} , it seems reasonable to expect that the optimum operating condition for the multiplier should be with the electric field across the undepleted epi no higher than that corresponding to the peak static electron velocity found from the Monte Carlo calculations. This is in the neighborhood of 4 to 5 kV/cm for donor concentrations above $1 \times 10^{17} \text{ cm}^{-3}$. Looking at the results of the MC simulations, the transient peak velocities are generally around 1.25 to 1.4 times the static velocities for those field strengths. For example, for a step of 5 kV/cm the electron velocity peaks at about $15.6 \times 10^6 \text{ cm/s}$, after which it decays to the static value around $11.0 \times 10^6 \text{ cm/s}$ in 4 or 5 ps, for a ratio of 1.4.

Output Frequency	Block Temperature	Simulation $N_D(\text{opt})$	Formula $N_D(\text{opt})$
200 GHz	300 K	$\leq 1 \times 10^{17}$	1.1×10^{17}
200 GHz	120 K	$\leq 1 \times 10^{17}$	0.5×10^{17}
400 GHz	300 K	$\approx 2 \times 10^{17}$	2.0×10^{17}
400 GHz	120 K	$\approx 1 \times 10^{17}$	1.0×10^{17}
800 GHz	300 K	$\geq 4 \times 10^{17}$	6.9×10^{17}
800 GHz	120 K	$\approx 3 \times 10^{17}$	3.2×10^{17}

Using these values, the peak velocities are in the neighborhood of 15 to $20 \times 10^6 \text{ cm/s}$ at room temperature, N_D between 10^{17} and 10^{18} cm^{-3} . At 120 K, the peak velocities are between 28 and $32 \times 10^6 \text{ cm/s}$, N_D being 5×10^{16} to $5 \times 10^{17} \text{ cm}^{-3}$. In this case, for illustration, the safety margin mentioned earlier will be dropped, and V_{BR} will be used for the PRV.

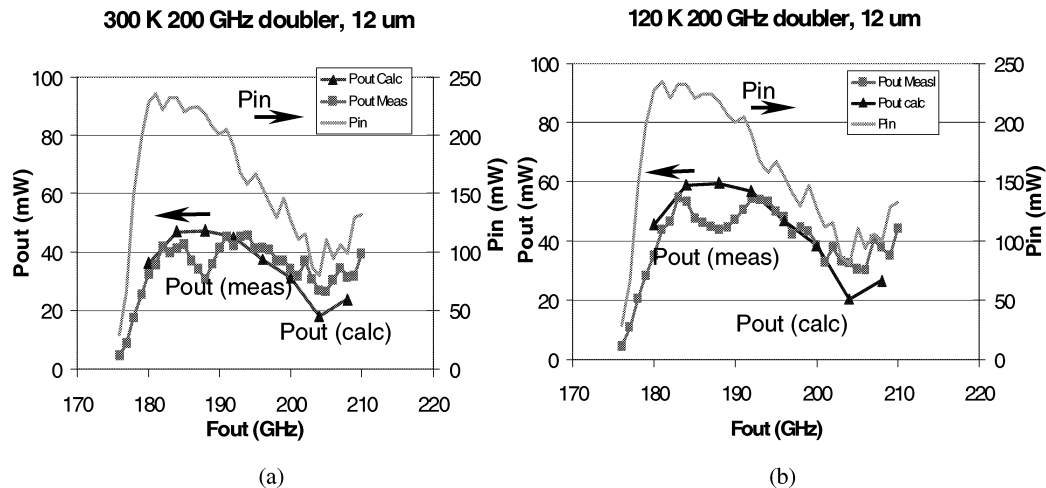


Fig. 7. Plots of measured and simulated 200 GHz doubler efficiency. The doping is $2 \times 10^{17} \text{ cm}^{-3}$. Anodes are $3 \times 12 \mu\text{m}$. Square symbols mark the measurements, triangles mark the simulations. (a) 300 K block temperature. (b) 120 K block temperature.

Table I compares the results from examining Figures 4 through 6 to those from the analytical formula. The agreement is good within the limits of what can be gleaned from the simulation plots.

V. DISCUSSION OF RESULTS OF IMPROVED MODEL COMPARED WITH MEASUREMENT

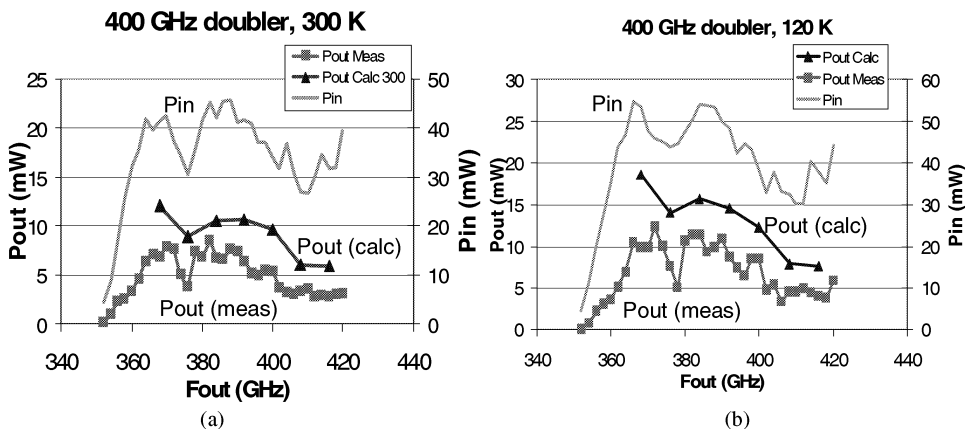


Fig. 8. Plots of measured and simulated 400 GHz doubler efficiency. The doping is $2 \times 10^{17} \text{ cm}^{-3}$. Anodes are $1.5 \times 4.5 \mu\text{m}$. Square symbols mark the measurements, triangles mark the simulations. (a) 300 K block temperature. (b) 120 K block temperature.

Using the same HB simulator, the existing designs for 200, 400 and 800 GHz doublers were also simulated. A representative photo of these designs appears in Figure 1. Three designs exist for the 800 GHz doubler [39], two variations of which include an on-chip MIM capacitor with Si_3N_4 for bias decoupling. The third variation was fabricated using a high-low transmission line low-pass bias filter. The 400 GHz doubler was only fabricated

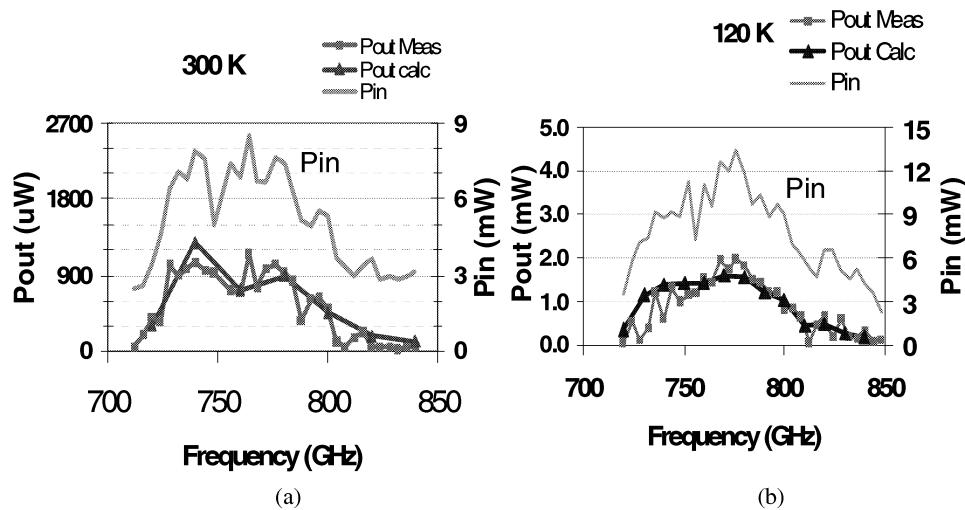


Fig. 9. Plots of measured and simulated 800 GHz doubler efficiency. The doping is $3 \times 10^{17} \text{ cm}^{-3}$. Anodes are $1 \times 1.2 \mu\text{m}$. Square symbols mark the measurements, triangles mark the simulations. (a) 300 K block temperature. (b) 120 K block temperature.

using the on-chip capacitor, whereas the 200 GHz doubler does its filtering with off-chip single-layer chip capacitors. The results of the simulations are compared to the measurements in Figures 7 through 9. The 800 GHz measured results for 120 K block

temperature have not been presented before, and represent the highest output power measured for an 800 GHz multiplier chain of which these authors are aware.

The agreement between measurement and calculation is good, with one exception: When the input power is high at the lower frequencies, the simulator overestimates the efficiency. This is clear, for example in the range of about 188 GHz for the 200 GHz doubler, and below 400 GHz for the 400 doubler. It appears as if the simulator is analyzing multiplier power saturation incorrectly. The 800 GHz doubler does not exhibit this behavior because it is not driven near saturation.

To confirm this, a power sweep measurement was performed on the 200 GHz doubler, along with the corresponding simulation. The results presented in Figure 10 confirm this problem. The agreement between simulation and measurement are good at the low power end, but the multiplier actually saturates at a lower input power and produces a lower output power than the simulator would predict.

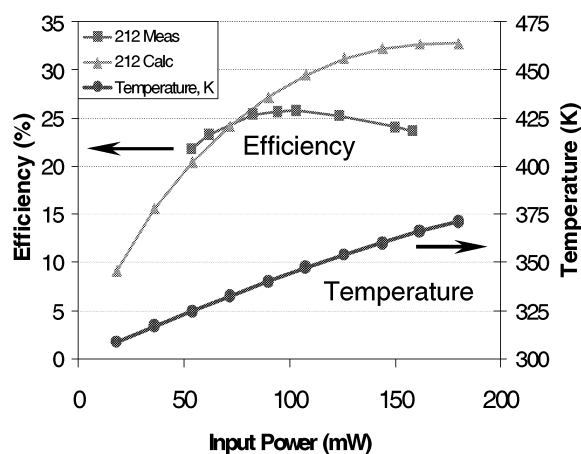


Fig. 10. Measured and simulated power sweep of the 200 GHz doubler. The frequency is 212 GHz. Square markers indicate the measurements, triangles indicate the simulation. Also shown is the simulated temperature.

An additional artifact of the modeling that appears in the optimization plots, especially Figure 6, is the kink at lower C_{j0} . This is due to a change in the width of the anodes at that point, give smaller diodes that can still be fabricated. The algorithm used to find the ohmic contact and spreading resistance for the rectangular diodes may be inaccurate for these small diodes. This needs to be investigated further.

VI. CONCLUSION

The improvements to the harmonic balance analysis and diode model that have been presented give results that match the measurements for 200, 400 and 800 GHz doublers very well. Further, low temperature measurements on one of the 800 GHz doublers have given a very high output power of 2 mW.

Nevertheless, there is room for improvement in the modeling, especially for multipliers running near saturation. Several possible improvements in the model will be tried. First, the way in which the harmonic balance simulator handles multipliers with several diodes will be made more realistic. Instead of assuming the power is equally divided, the diodes will receive power as determined by the circuit used, accounting for the coupling between them.

Second, at high input power there is some effect that is not accounted for. For example, the reverse current electrons at high reverse bias have a great deal of energy with respect

to the material in the undepleted epi. One could surmise that these electrons will also stay in the upper low-mobility valleys, and may in fact increase the series resistance without being part of the normal high-field current saturation mechanism. These possibilities will be investigated in further studies, including the further application of Monte Carlo methods.

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