Multi-Anode Frequency Triplers at Sub-Millimeter Wavelengths

Alain Maestrini, Charlotte Tripon-Canseliet, John Ward, Hamid Javadi, John Gill, Goutam Chattopadhyay, Erich Schlecht, and Imran Mehdi

***Abstract*—We report on the design methodology of fix-tuned split-block waveguide balanced frequency triplers working at 300, 600 and 900 GHz. They feature four to six GaAs Schottky planar diodes in a balanced configuration. A 6-anode 300 GHz tripler, a 6-anode 560 GHz tripler and a 4-anode 900 GHz circuits will be fabricated with JPL membrane technology in order to minimize dielectric load and insure an accurate thickness of the substrate. A 4-anode 600 GHz tripler is already fabricated with JPL substrate-less technology and delivers 0.8-1.6mW in the 540-640 GHz band at room temperature. When cooled to 120K this tripler delivers 2-4mW in the 540-640 GHz.**

***Index Terms*—local oscillator, varactor, Schottky diode, frequency multiplier, frequency tripler, submillimeter wavelength.**

I. Introduction

WIDE BAND frequency triplers with high efficiency are highly desirable to build THz sources based on a cascade of frequency multipliers: for the same output frequency, less stages are required with triplers than with doublers. A demonstration of the feasibility of a ×2×3×3 chain in the band 1.7-1.9 THz have already been presented in [1]. The present paper will discuss the design methodology of wide-band multiple anode triplers. Focus will be put on a 260-340 GHz fixed-tuned tripler that will be used as the first stage of a future ×3×3×3 chain to 2.7 THz. Similar multipliers have been designed for higher frequencies: a 6-anode 510-590 GHz tripler and a bias-able 4-anode 900 GHz tripler that will be used as the second stage of a future 2.7 THz chain. The circuits of these multipliers are currently being fabricated at JPL Micro Device Laboratory. A 4-anode 540-640 GHz balanced tripler is already fabricated with JPL substrate-less technology and delivers 0.8-1.6mW in the 540-640 GHz band at room temperature [2].

II. Accurate 3D modeling of the multipliers

Since the mid-90's works of Tuovinen, Erickson [3] and Hesler [4] on the design of millimeter and submillimeter-wave multipliers and mixers using commercial 3D field solvers such as Ansoft HFSS, the accuracy of the calculations has been greatly enhanced, in part by the improvement of the codes themselves but much more by the multiplication by a factor 10 to 20 of the capacity of the memory-chips and the speed of the CPUs. It is now possible to resolve very fine details of the multipliers with a ratio in excess of 1:10,000 between the smallest and the bigger dimension. This capability is of prime importance to model details such as the passivation layers which thickness typically ranges between 0.1 and 0.3 μm, depending on the process, or to model the air-bridges which are of only one to a few micrometers wide. The other dimensions of the circuit can reach a millimeter or more. The definition of the micro-coaxial probe, used as an Ansoft HFSS wave-port to measure the fields and calculate the impedance seen at the exact location of the Schottky contact [4], requires also very fine details.

In our model we included the passivation layers and we set the gap between the inner and the outer conductor of the micro-coaxial probe to 0.1 μm. This had the effect to model accurately the parasitic capacitance of the Schottky diode.

III. Topology and design steps for wide band frequency triplers

1. Topology: the triplers are split-block waveguide designs that feature four to six Schottky planar varactor diodes, monolithically fabricated on a GaAs-based substrate (3 to 5 μm-thick membrane or 12 μm-thick substrate) and connected in series at DC (see Fig. 1). The chips are inserted between the input and the output waveguides in a channel. An E-plane probe located in the input waveguide couples the signal at the fundamental frequency to a suspended microstrip line that can propagate only a quasi or true TEM mode (depending on the design, dielectric is or is not present in the channel). This line has several sections of low and high impedance used to match the diodes at the input and output frequency and to prevent the third harmonic from leaking into the input waveguide. The third harmonic produced by the diodes is coupled to the output waveguide by a second E-plane probe.

Inside the chip-channel, the circuit is quasi-symmetrical (small asymmetries are introduced by the physical structure of the Schottky diodes). Given the symmetry of the excitation, the odds harmonics are generated on a TEM mode and the even harmonics are trapped in a virtual loop (the line of diodes) provided that the suspended microstrip line cuts-off the parasitic TE mode. More detail about this topology can be found in [5].

A. Maestrini is with Laboratoire des Instruments et Systèmes d'Ile de France - Université Pierre et Marie Curie, 4 place Jussieu, case 252, 75252 Paris cedex 5, France, and is associated with Laboratoire d'Etude du Rayonnement et de la Matière en Astrophysique, Observatoire de Paris, France. Email : alain.maestrini@lisif.jussieu.fr

J. Ward, J. Gill, H. Javadi, E. Schlecht, G. Chattopadhyay, I. Mehdi are with the Jet Propulsion Laboratory, California Institute of Technology, MS 168-314, 4800 Oak Grove Drive, Pasadena, CA 91109, USA.

C. Tripon-Canseliet is with LISIF - Université Pierre et Marie Curie, France.

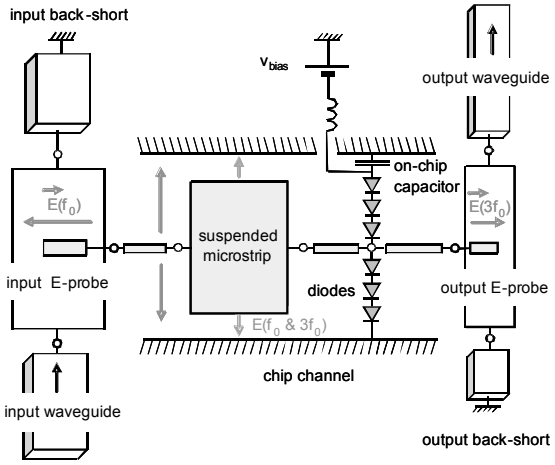

Fig. 1: block diagram of the 300 GHz balanced tripler. Inside the chip channel, only a quasi-TEM mode can propagate at all the frequencies of interest.

2. Design method: detailed explanations of the design methodology are given in [2]. In summary, the first step is to optimize the diodes cell that consists in the part of the circuit that includes the diodes, a section of the chip-channel and two sections of the propagating line at the center of the chip (see Fig. 2). The optimization is performed using 3D electromagnetic codes like Ansoft HFSS and harmonic-balance codes like Agilent ADS. The optimum diode junction capacitance and bias voltage is also determined at the same time.

This optimization is performed for a given input power and output frequency. The doping level is crucial because it defines the breakdown voltage which is the main parameter that controls the power handling capability per anode. Time domain non-linear simulations have been performed to check the waveform of the voltage across the diodes in order to determine the maximum input power and optimum bias voltage. For our 6-anode 300 GHz tripler and our 6-anode 560 GHz tripler the doping level is set to 2^E17 cm^{-3} that allows 70 to 80 mW of input power to be safely handled. The doping for the 4-anode 600 GHz is 1^E17 cm^{-3} that allows 100 to 120 mW to be safely handled. For the 4-anode 900 GHz tripler the doping is 5^E17 cm^{-3} and therefore only about 15 to 18 mW can be handled.

The second step is to optimize the input and output matching circuit using on-chip and waveguide matching elements. This is done by first optimizing the circuit at the center of the band of interest using non-linear simulations. A minimum of matching elements is used. The bandwidth is then extended by adding to the input and output waveguides a succession of sections of high and low impedances. As the matching circuit in the input and output waveguide are independent, it is possible to use linear simulations.

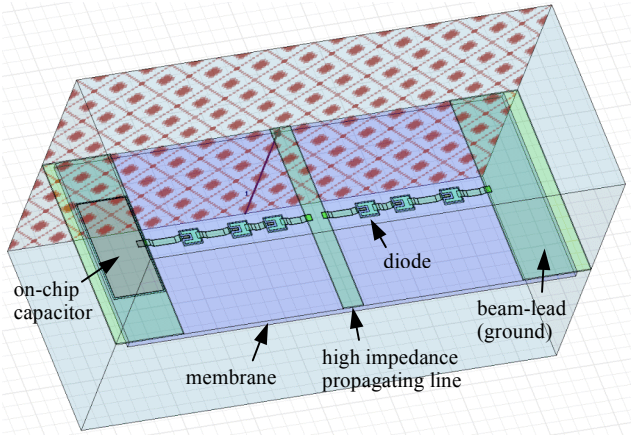

Fig. 2: diodes cell used to optimize the channel cross-section dimensions, the location of the 6 anodes and the air-bridge size. One of the HFSS ports is shown in the back side of the diode cell.

3. Design of a high efficiency wideband 300 GHz tripler: using this methodology, we designed a high power 6-anode 260-340 GHz tripler to be used as the first driver of a 2.7 THz LO chain (see Fig. 3). The expected peak efficiency is 12% at room temperature with a -3dB bandwidth of 25%. A very good balance between the diodes at the input and the output frequencies has been successfully achieved (see Fig. 4). The performance is expected to greatly increase upon cooling: at 120K ambient temperature, the conversion efficiency of the multiplier is expected to reach 20% at 300 GHz.

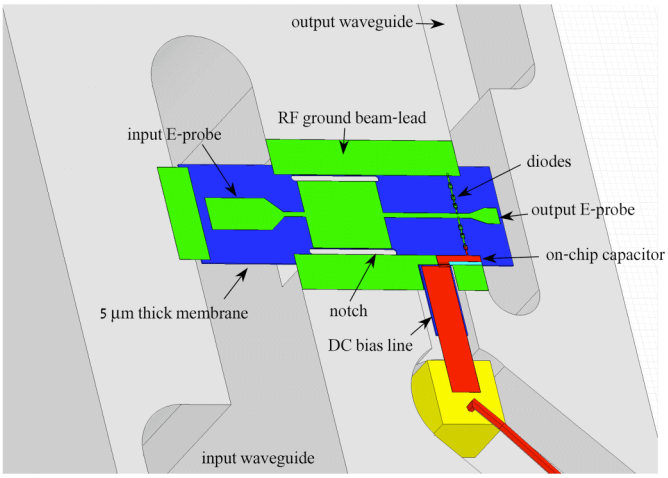

Fig. 3: 3D view of the bottom part of the waveguide block with the 260-340GHz tripler chip installed. The device is fabricated on a 5µm thick GaAs membrane substrate. It features 6 Schottky diodes in a balanced configuration. The chip is hold by two beam leads. An on-chip capacitor is used to reverse-bias the anodes. The complete input matching waveguide-circuit (cutoff in the figures) consists of several reduced-height rectangular waveguide sections and several standard-height rectangular waveguide sections. The waveguide backshorts and steps are not represented to their optimized positions.

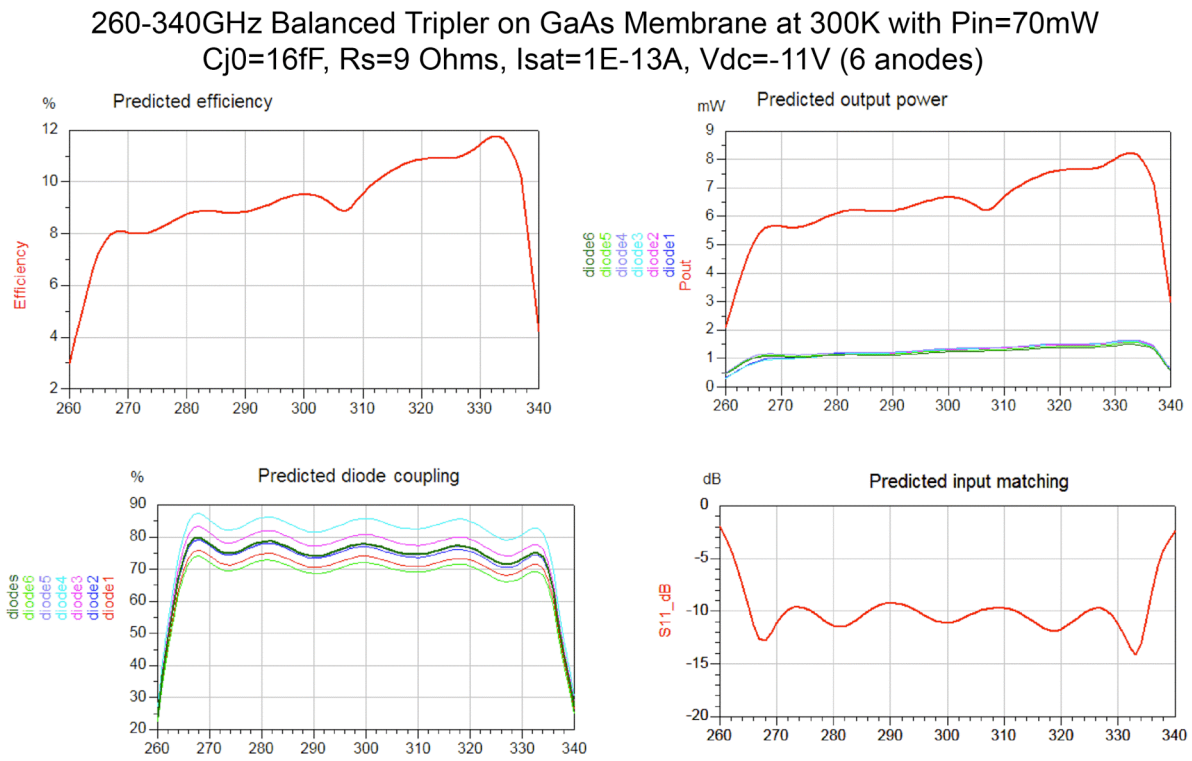

Fig. 4: Predicted performance of the 6-anode 260-340GHz balanced tripler at room temperature with 70 mW of input power. When cooled to around 120K the conversion efficiency of the multiplier is expected to reach 20% at 300 GHz. The coupling at the input frequency is calculated for each diode (left and bottom curves). The calculated output power per diode is shown on the right and top curves along with the total output power.

Conclusion

In recent years, tremendous progress has been made in the design methodology and the fabrication of submillimeter Schottky diode-based circuits. We recently demonstrated a wideband high power 540-640 GHz balanced tripler which concept was used to design a family of balanced triplers using up to 6 anodes and for frequencies ranging from 300 GHz to 900 GHz.

Acknowledgements

The authors are grateful for the helpful technical discussions with Dr. Peter Siegel and Dr. John Pearson and for the superb fabrication of the 540-640 GHz waveguide blocks by James Crosby and the JPL Space Instruments Shop.

References

[1] A. Maestrini, J. Ward, J. Gill, H. Javadi, E. Schlecht, G. Chattopadhyay, F. Maiwald, N.R. Erickson, and I. Mehdi, "A 1.7 to 1.9 THz Local Oscillator Source," *IEEE Microwave and Wireless Components Letters*, Vol. 14, no. 6, pp. 253-255, June 2004.

[2] A. Maestrini, J. Ward, J. Gill, H. Javadi, E. Schlecht, C. Tripon-Canseliet, G. Chattopadhyay and I. Mehdi, "A 540-640 GHz High Efficiency Four Anode Frequency Tripler", to be published in IEEE-MTT, 2005.

[3] J. Tuovinen, N.R. Erickson, "Analysis of a 170 GHz frequency doubler with an array of planar diodes," *IEEE Trans. Microwave Theory Tech.*, Vol. 43, no. 4, pp. 962–968, April 1995.

[4] J. Hesler, "Planar Schottly diodes in submillimeter-wavelength waveguide receivers", Ph.D. dissertation, faculty of the School of Engineering and Applied Science, University of Virginia, January 1996.

[5] S.A. Maas, "Non-linear Microwave Circuits, Artech House, 1988.