

# A High Efficiency Multiple-Anode 260-340 GHz Frequency Tripler

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**Abstract**— We report on the fabrication at the Jet Propulsion Laboratory of a fixed-tuned split-block waveguide balanced frequency tripler working in the 260-340 GHz band. This tripler will be the first stage of a  $\times 3 \times 3 \times 3$  multiplier chain to 2.7 THz (the last stages of which are being fabricated at JPL) and is therefore optimized for high power operation. The multiplier features six GaAs Schottky planar diodes in a balanced configuration integrated on a few  $\mu\text{m}$ -thick membrane. Special attention was put on splitting the input power as evenly as possible among the diodes in order to ensure that no diode is over-driven. Preliminary RF tests indicate that the multiplier covers the expected bandwidth and that the efficiency is in the range 1.5-7.5 % with 100 mW of input power.

**Index Terms**— Local oscillator, varactor, planar diode, Schottky diode, frequency multiplier, frequency tripler, balanced tripler, submillimeter wavelengths.

## I. INTRODUCTION

Frequency multiplication offers the possibility to create tunerless compact frequency-agile terahertz sources working at room temperature that are well-suited to pump Hot Electron Bolometer (HEB) mixers [1],[2]. Nevertheless, there has been no demonstration of a fully solid-state local oscillator at frequencies above 1.95 THz. This limitation is due in part to the lack of drive power in the 600-1200 GHz range, which can in turn be traced to the power available in the 200-400 GHz range. The purpose of the current work is to create a wideband 300 GHz source with sufficient output power to be used as a first stage of a  $\times 3 \times 3 \times 3$  chain to 2.7 THz.

## II. DESIGN & FABRICATION

A preliminary design of the balanced 260-340 GHz tripler along with the predicted performance have been presented in [3]. The tripler is a split-block waveguide design that features six Schottky planar varactor diodes, monolithically fabricated on a  $\sim 5 \mu\text{m}$ -thick GaAs membrane. The chip is

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mounted in a channel that runs between the input and the output waveguides (see Fig. 1).

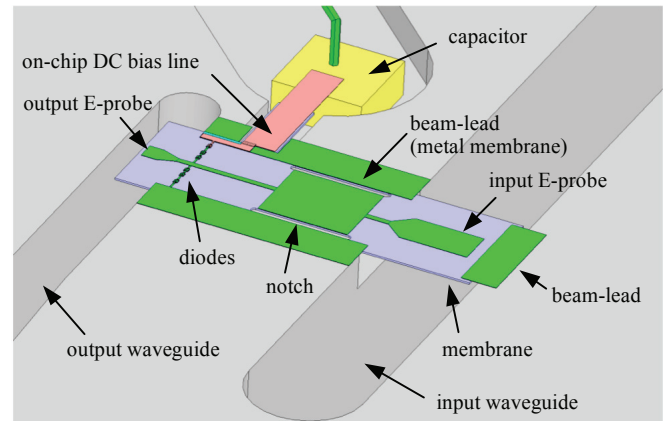


Fig. 1. 3D view of the bottom part of the waveguide block (partial view) with the 300 GHz tripler chip. The device is fabricated on a  $5 \mu\text{m}$  thick GaAs membrane substrate. It features six Schottky diodes in a balanced configuration. The total length of the device is about 1 mm.

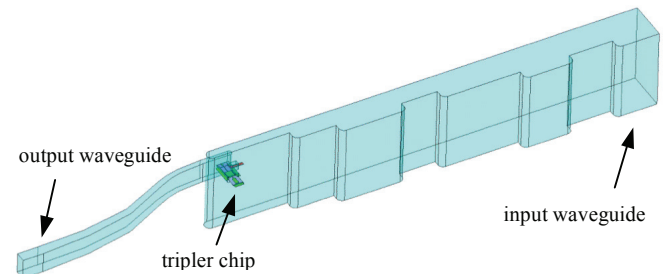


Fig. 2. 3D view of the entire 260-340 GHz frequency tripler. The total length of the matching circuit in the input waveguide is about 14 mm. The total length of the circuit is 20 mm.

An E-plane probe located in the input waveguide couples the signal at the fundamental frequency to a suspended microstrip line. This line has several sections of low and high impedance used to match the diodes at the input and output frequencies and to prevent the third harmonic from leaking into the input waveguide. The third harmonic produced by the diodes is coupled to the output waveguide by a second E-plane probe. The bandwidth of the multiplier was extended by adding to the input waveguide a succession of sections of high and low impedances [3]. With respect to the design presented earlier, the current design uses exactly the same device, but the waveguide input matching network has been slightly modified and the step in the output waveguide has been removed. The predicted performance of the final circuit are very similar to those published in [3].

Fig.1 shows a schematic of the 260-340 GHz tripler chip while Fig. 2 shows a schematic of the entire multiplier.

Fig. 3 shows two pictures of a tested multiplier. Note that the output probe on this particular chip is defective: it is only 50  $\mu\text{m}$  long instead of 90  $\mu\text{m}$ . At the time this paper was written, this was the only device available for testing.

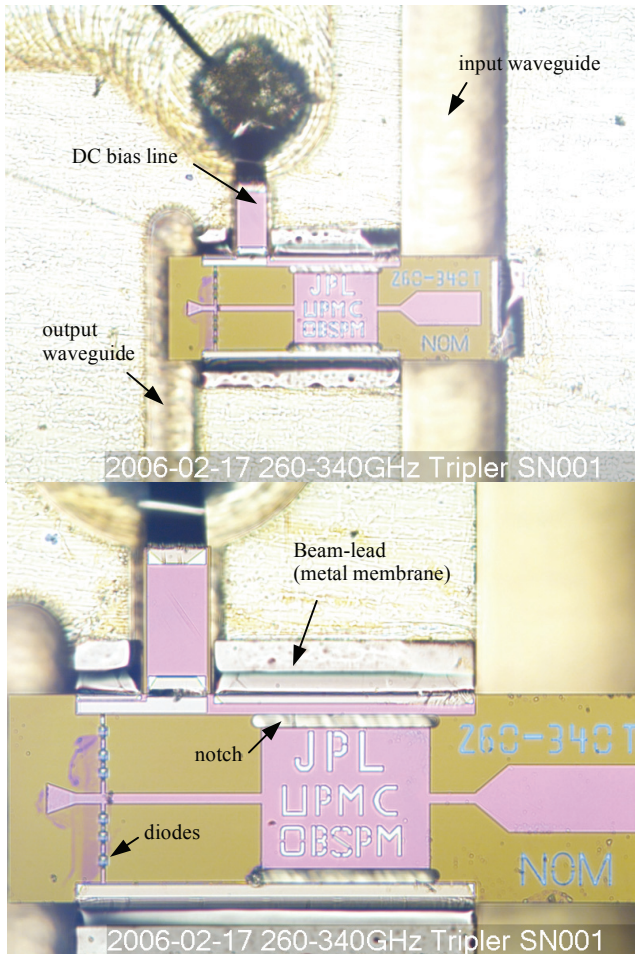


Fig. 3. Photograph of the bottom part of the waveguide block with a 300 GHz tripler chip and the DC capacitor installed (top). Detail of the 260-340 GHz tripler chip (bottom). NOTE that the output probe on this particular chip is defective: it is only 50  $\mu\text{m}$  long instead of 90  $\mu\text{m}$  (compare with the 3D schematic of Fig. 1).

### III. PRELIMINARY MEASUREMENTS

The output power of the 260-340 GHz tripler was measured at room temperature using an Erickson Instruments PM3 power meter [4] and a one-inch long WR10 to WR3 waveguide transition. No corrections were made for the losses in the waveguide transition. Fig. 4 shows the output power and the conversion efficiency across the band while keeping the input power at 100 mW (except near the edges of the band). The bias was optimized for each frequency point. Despite the defective output probe, this multiplier shows excellent performance and covers the entire band 260-330 GHz band. Due to limitations of the W-band drive source, no measurements were made above 330 GHz, so it is not clear if the multiplier does actually reach 340 GHz as predicted.

The efficiency of the multiplier as a function of the input power was measured at room temperature by varying the

input power from 3 mW (+4.8 dBm) to 192 mW (+22.8 dB) while optimizing the bias at each input power level (see Fig. 5). The output frequency was fixed at 318 GHz where the efficiency was close to the maximum and where almost 200 mW of drive power was available. Fig. 5 shows that the efficiency saturates at relatively low input power (+9 dBm = 8 mW) and decreases with the increasing input power above +9 dBm. This decrease of the efficiency becomes more noticeable for input power levels above +17 dBm (50 mW). This may indicate that the diodes are overheating due to the thin substrate under the diodes. No thermal study has been performed yet to verify this hypothesis.

Simulations were performed to estimate the impact of the flawed output probe (see Fig. 6). The 3D structure of the actual multiplier was re-simulated with a finite-element EM-solver (Ansoft HFSS V10.1). Fig. 6 shows the predicted performance of the defective chip biased with the same DC voltage and pumped with the same input power as the measurements. The results of this simulation are compared to the measurements in Fig. 6. The difference between measurements and predictions is in the range -3.2 dB to -1.2 dB (excluding a relatively narrow resonance around 300 GHz). It is important to note that these simulations were performed with the same set of parameters (series resistance, intrinsic junction capacitance, metallic losses, etc.) as the one used for the optimization of the circuit [3]. No retro-fit has been made. Since only one chip has been tested, it is impossible to say at this point if the initial predicted efficiency will be matched with a better chip, but it does appear likely that the predicted bandwidth will be achieved.

Fig. 6 also shows the predicted performance of the multiplier with a normal chip when pumped with a flat input power of 100 mW and when biased with a voltage of -13V. The same simulation is performed by replacing the normal chip by the defective chip. These simulations indicate that the performance of the multiplier should improve noticeably when a non-defective chip is mounted into the waveguide block. An increase of at least +3dB with respect to the measurements is expected for the lowest frequencies while an increase of at least +1dB is expected at the high end of the band.

### IV. CONCLUSION

The preliminary results presented in this paper show that Schottky frequency triplers operating at 300 GHz can have both wide electronically-tunable bandwidth and high conversion efficiency. On-going research at the Jet Propulsion Laboratory in collaboration with the Université Pierre et Marie Curie-Paris 6 and the Observatoire de Paris focuses now on power-handling and power combining to increase the power produced at 300 GHz.

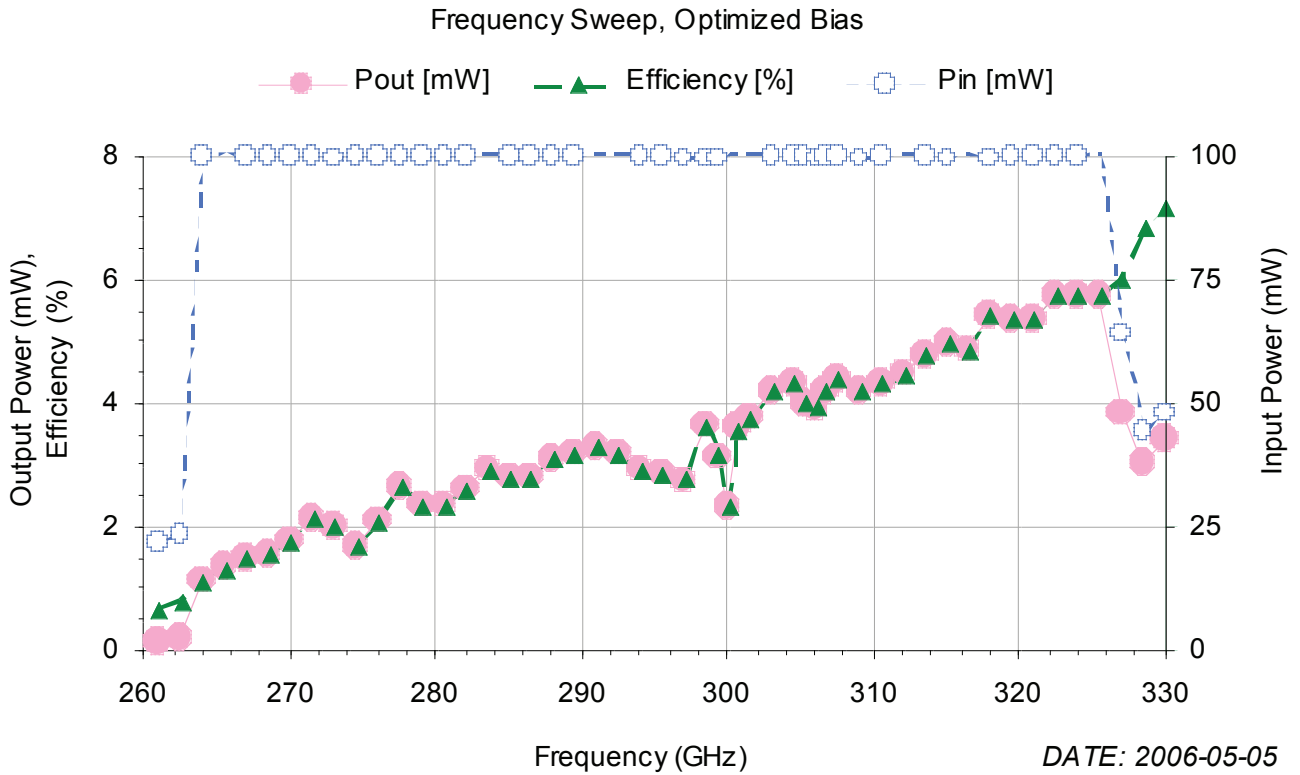


Fig. 4. Frequency sweep across the 260-330 GHz band. Input power is kept constant except at the edge of the band due to the roll-off of the W-band power amplifiers used for the measurements.

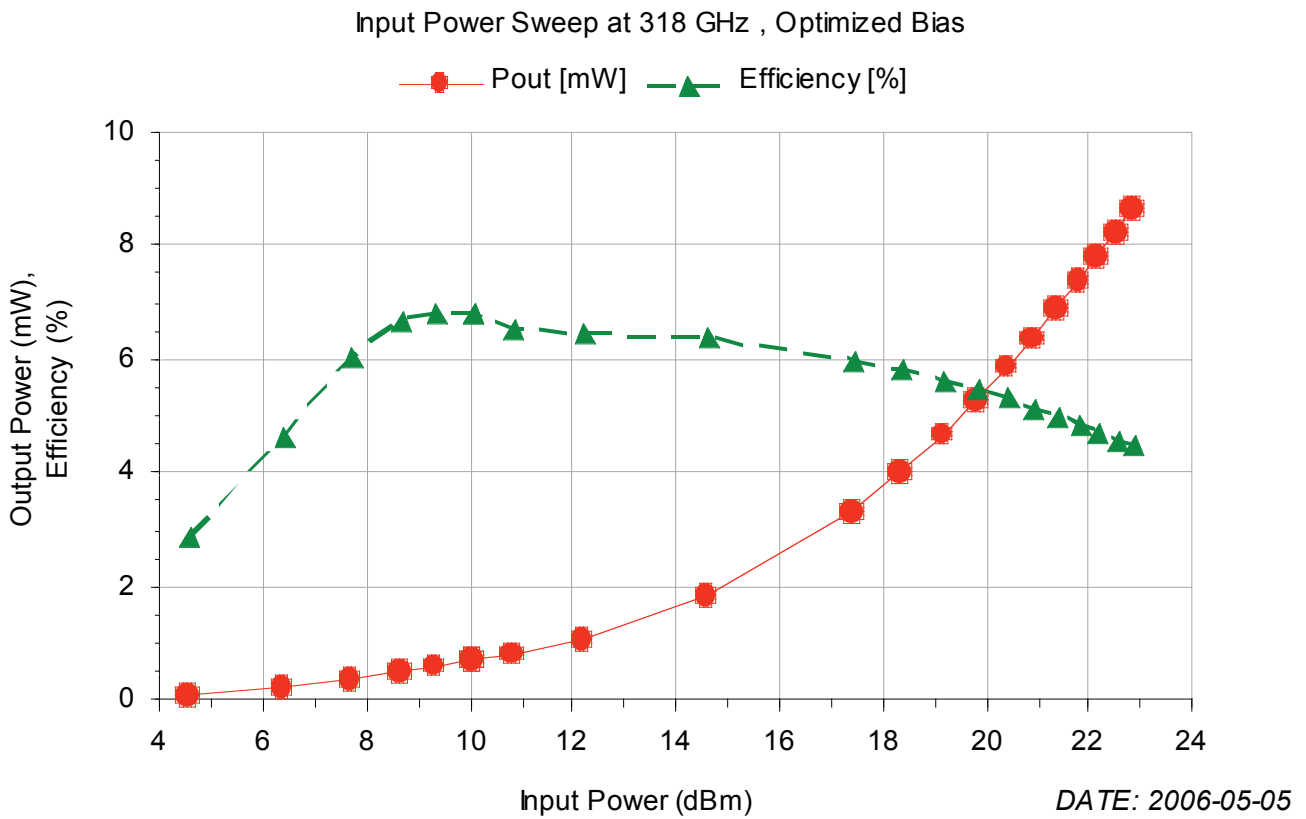


Fig. 5. Power sweep at the output frequency of 318 GHz. The bias is optimized for each input power level.

## Measurements vs. Simulations at Room Temperature

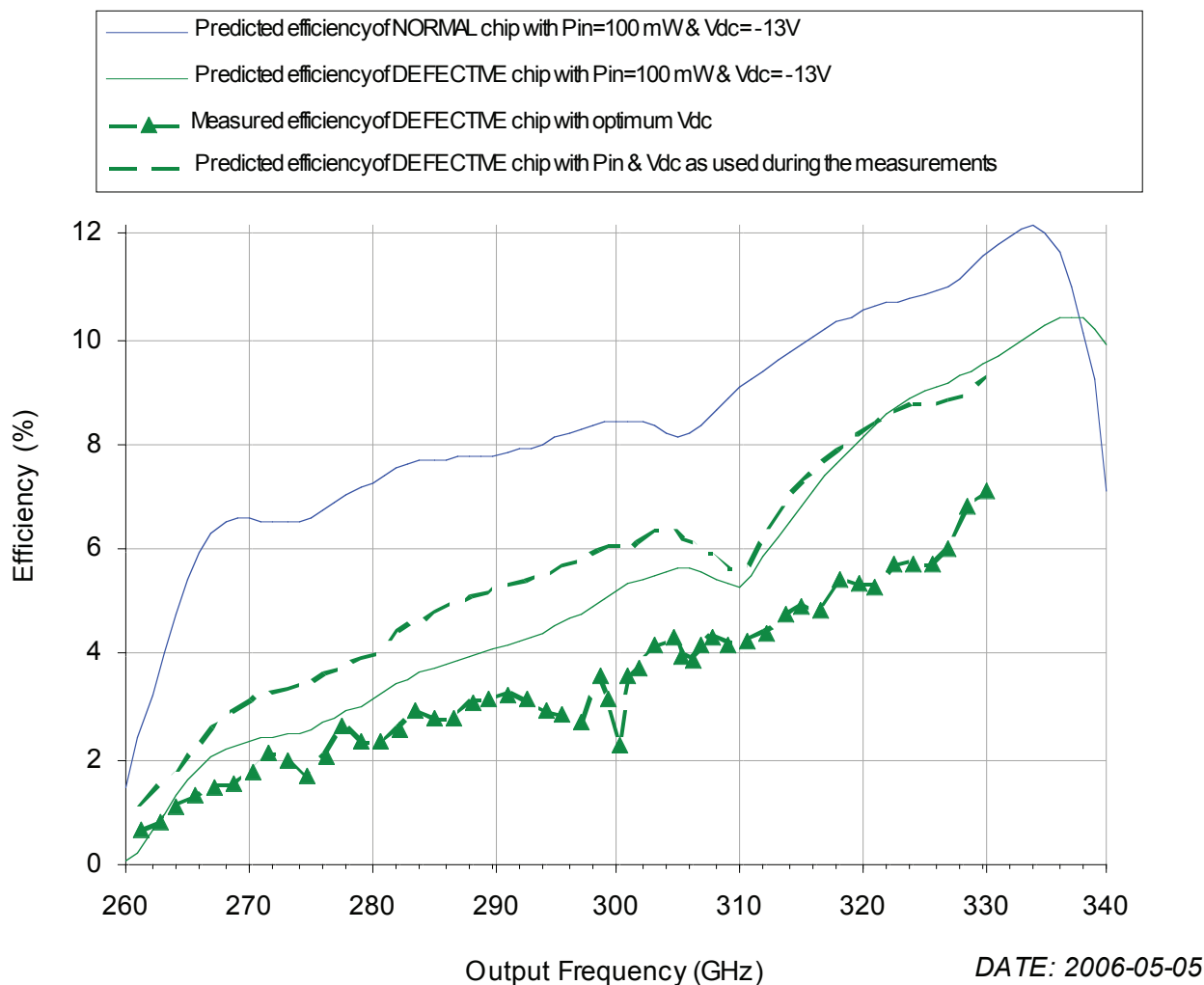


Fig. 6. Simulated efficiency versus frequency compared to the measured efficiency of the 260-340 GHz tripler.

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