Local Oscillator Chain for 1.55 to 1.75 THz With 100-μW Peak Power

Alain Maestrini, John S. Ward, Hamid Javadi, Charlotte Tripon-Canseliet, John Gill, Goutam Chattopadhyay, Erich Schlecht, and Imran Mehdi

***Abstract*—We report on the design and performance of a fix-tuned $\times 2 \times 3 \times 3$ frequency multiplier chain that covers 1.55–1.75 THz. The chain is nominally pumped with 100 mW at W-band. At 120 K the measured output power is larger than 4 μW across the band with a peak power of 100 μW at 1.665 THz. A similar chain operated at room temperature produced a peak power of 21 μW. These power levels now make it possible to deploy multipixel heterodyne imaging arrays in this frequency range.**

***Index Terms*—Frequency multiplier, frequency tripler, local oscillator (LO), Schottky diode, submillimeter wavelength, THz technology, varactor.**

I. Introduction

The 1.4 to 1.9 THz band includes a number of astronomically significant spectral lines that will be targeted by ground based, air-borne and space-borne observatories [1]. The Jet Propulsion Laboratory (JPL) has led a concerted effort toward developing and deploying compact solid state sources in this frequency range. A compact solid state source based on cascaded frequency doublers working in the 1.4 to 1.6 THz range has been previously demonstrated [2]. Similarly, preliminary results obtained from a $\times 2 \times 3 \times 3$ chain in the 1.7 to 1.9 THz range that produced a peak of 15 μW at 120 K have also been reported [3]. Both of these chains provide more than enough power to pump hot electron bolometer (HEB) mixers [4]. However, neither chain was able to provide usable power from 1.6 to 1.7 THz, leaving a large gap in frequency coverage. This letter will present recently obtained results in this previously uncovered band. An upgraded device model and second generation circuit synthesis have allowed us to improve efficiency and output power relative to previous results as well as accurately achieve the required frequency tuning. The third (final) stage tripler of this chain is based on the same chip design as used for the corresponding stage of the previous 1.7–1.9 THz chain, except with larger anodes, while the second stage was replaced with a new, high power, high efficiency 4 anode tripler. New waveguide tuning circuits based on the improved device modeling allowed us to obtain state-of-the-art results in the 1.55–1.75 THz band. We have now covered the entire 1.41–1.91 THz band with only three different local oscillator (LO) chains with sufficient LO power to deploy multi-pixel imaging arrays.

Manuscript received June 17, 2005; revised September 20, 2005. This work was supported by the Jet Propulsion Laboratory, California Institute of Technology under a contract with the National Aeronautics and Space Administration. The review of this letter was arranged by Associate Editor F. Ellinger.

A. Maestrini is with the Laboratoire des Instruments et Systèmes d'Ile de France (LISIF), Université Pierre et Marie Curie, Paris 75252, France. He is also with the Laboratoire d'Etude du Rayonnement et de la Matière en Astrophysique, Observatoire de Paris, Paris, France (e-mail: alain.maestrini@lisif.jussieu.fr).

J. S. Ward, J. Gill, H. Javadi, E. Schlecht, G. Chattopadhyay, and I. Mehdi are with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA (e-mail: john.ward@jpl.nasa.gov).

C. Tripon-Canseliet is with the Laboratoire des Instruments et Systèmes d'Ile de France (LISIF), Université Pierre et Marie Curie, Paris 75252, France.

Digital Object Identifier 10.1109/LMWC.2005.859989

II. Improved Drive Stage and Device Modeling

The 1.7–1.9 THz chain described in [3] is based on a $\times 2 \times 3 \times 3$ configuration. The second stage multiplier, a tripler to 600 GHz implemented with 2 anodes in a balanced configuration, proved to be limiting in terms of bandwidth, power handling, and efficiency. To ease these limitations, we designed and implemented a novel 540–640 GHz tripler using four anodes for improved power handling and tuned for high efficiency and bandwidth. When operated at 120 K this tripler produces approximately 3 mW across the 545–640 GHz band with a peak of 4.2 mW at 630 GHz [5], providing adequate power to optimally pump the third and final stage of the LO chain.

Planar integrated circuits fabricated at JPL are passivated with a silicon dioxide layer. This passivation layer is nominally a few hundred nanometers thick. In earlier simulations this passivation layer was neglected. However, in recent simulations it was discovered that for chips working above a terahertz this seemingly thin dielectric layer can have a large impact on the circuit performance. Thus, a new three-dimensional (3-D) model has now been incorporated into the electromagnetic (EM) simulation that accurately models the passivation layer. Moreover, the definition of the micro-coaxial probes, used as wave-ports to measure the impedance at the exact location of the Schottky contacts, was refined [5]. For each diode, the anode itself defines the inner conductor; the outer conductor is defined by the edges of a small rectangle that lies on the top face of the mesa around the anode. The gap between the edges of the anode and this rectangle was set to about 0.1 μm compared to 0.4 μm for previous simulations. These modifications have the effect of more accurately modeling the parasitic capacitance of the Schottky diode, allowing one to precisely target the frequency band of interest. This new model was utilized to design the final stage tripler of the chain.

III. Final Stage Tripler Design

With the improved device model it is now possible to more accurately predict the response of the tripler devices as a function of frequency and input power. The tripler devices used in

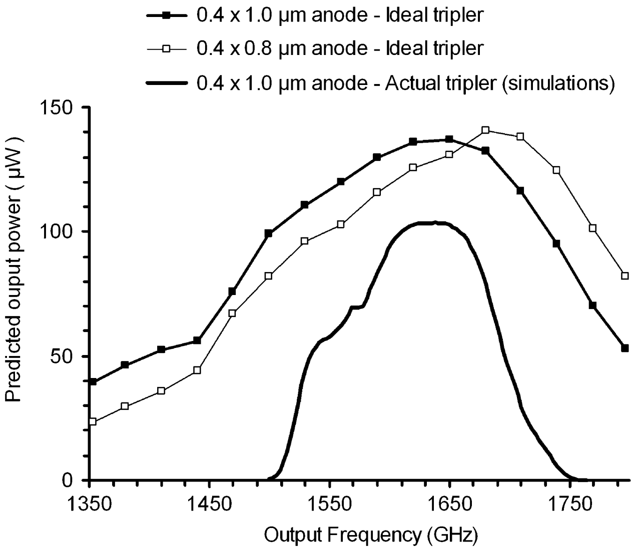

Fig. 1. Predicted intrinsic response of the last stage tripler chip with 5-mW input power is shown for two different anode sizes and an ambient temperature of 120 K. The final stage tripler response simulation for the actual tripler design including waveguide tuning circuits is shown at the same input power and temperature.

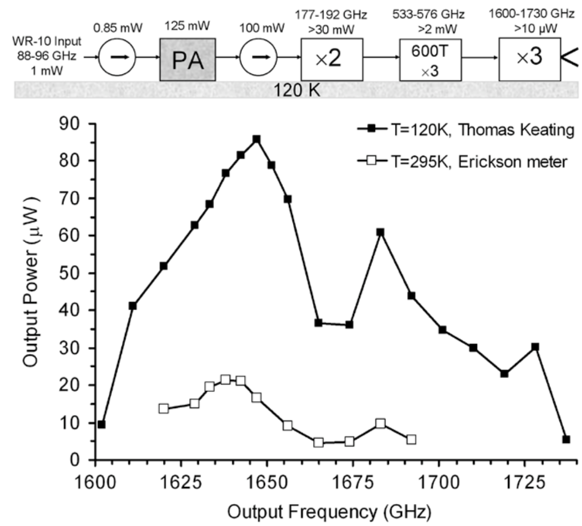

Fig. 2. Schematic (top) and performance (bottom) of the 1600–1735 GHz LO chain that was constructed from the 540–640 GHz drive stage and a redesigned last stage tripler. Results were measured at 120 K (black square curve and at room temperature (white square curve).

the 1.7–1.9 THz chain have been described previously in [3], [6]. The optimum device for that band has an anode size of 0.4 μm $\times$ 0.8 μm. A number of devices with different anode sizes were fabricated on the same GaAs wafer. The intrinsic response of the tripler chip was first investigated via simulations. This is shown in Fig. 1 as the "ideal tripler" for two anode sizes and 5 mW of input power at an ambient temperature of 120 K. In this particular case the input and output matching circuits for the chip were optimized for each frequency by adjusting the position of the input and output waveguide backshorts and waveguide steps. This provides insight into the intrinsic response of the chip. As can be seen in Fig. 1 the chips have fairly broad bandwidth and can cover the desired frequency range. For the 1.55–1.75 THz band the optimum response is obtained from the chip with a slightly larger anode (0.4 μm $\times$ 1.0 μm, doping 5×10^{17} cm^{-3}). The large intrinsic bandwidth is partly due to the fact that only a few matching elements are implemented on-chip and most of the input and output matching circuit is realized in low-loss waveguide.

Finally, a new waveguide block was designed and fabricated to be optimally tuned to cover the band of interest. This simulation is also shown in Fig. 1, labeled as the "actual tripler." It can be seen that the achieved simulated peak power of the actual tripler is about 25% lower than the simulated peak power of the intrinsic response of the chip and that the bandwidth is greatly reduced. The reasons are twofold: first, the input matching circuit was optimized for the 1.55–1.71 THz band. Secondly, the output matching circuit is optimized for 1650 GHz but contains only a waveguide backshort and a single waveguide step which is not enough to achieve wide band operation for this chip. While in principle a multisection output tuning circuit could have been designed to provide increased bandwidth, in practice such a circuit would be extremely difficult to fabricate with conventional machining given the small dimensions required for this frequency band.

As in [3] and [6], the last stage frequency tripler has the output waveguide dimensioned to cut off any signal at the second harmonic of the pump signal. This waveguide is transitioned to a built-in diagonal feed horn with a -3 dB beam width of 10°.

IV. RESULTS

The method used to measure the output power of the multiplier chains was presented in [3]. At room temperature, the power generated by the multiplier chain was measured with an Erickson calorimeter [7]. A transition from circular to WR10 rectangular waveguide was connected at the output of the built-in diagonal horn of the last multiplier. No correction was made for the loss of this transition. At cryogenic temperatures the output power is measured quasioptically with a Thomas Keating power meter [8].

A schematic of the first chain constructed to cover the 1.6–1.7 THz band is shown in the top half of Fig. 2. This chain utilizes the four-anode 540–640 GHz second stage tripler mentioned previously, which provides high power in-band but causes a low-frequency roll off at 1600 GHz. Both room temperature and 120 K results are shown. At 120 K peak power of 86 μW was measured with at least 10 μW available from around 1600 to 1735 GHz. At room temperature the chain delivers more than 5 μW in the 1620 to 1695 GHz band with peak power of 21 μW at 1640 GHz.

A second chain was constructed where the second stage tripler was replaced with a newly designed tripler that covers the 510–590 GHz range with higher output power. The schematic of this chain is shown in Fig. 3. A Golay cell with a diamond window was also used for the output power measurement at 120 K. Its total responsivity, which corresponds to its intrinsic responsivity multiplied by the optical coupling efficiency, was calibrated against the Thomas Keating power meter at one frequency. Fig. 3 shows the output power measured by the Golay cell and the Thomas Keating meter. The chain

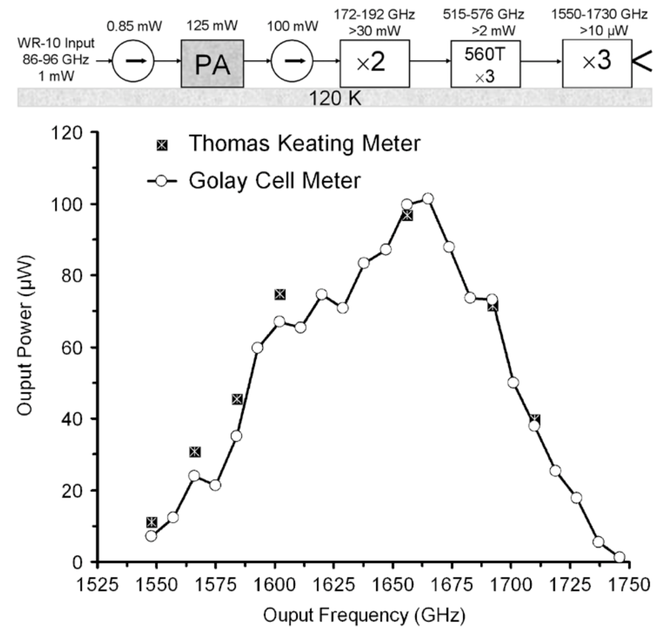

Fig. 3. Schematic (top) and performance (bottom) of the 1550–1750 GHz chain constructed with a new 510–590 GHz driver and a redesigned last stage tripler.

produces at least 10 μW in the 1550–1735 GHz band with a measured peak power of 100 μW at 1660 GHz.

V. Conclusion

We have demonstrated a complete LO chain to cover the 1.55 to 1.75 THz range with well-optimized efficiency and output power. Measurements show a peak power of 100 μW, a -3 dB bandwidth of $\sim$6.5% and a -10 dB bandwidth of 11% at 120 K. The targeted bandwidth was perfectly matched with power levels well in excess of the needs of a single pixel HEB heterodyne receiver. These results open the possibility to pump an array of HEB mixers in this frequency range with a single LO. Simulations indicate that the intrinsic response of the chip used in the last stage multiplier is much wider than the bandwidth of the current multiplier, allowing different power-versus-bandwidth compromises.

Acknowledgment

The authors wish to thank the staff of the JPL Space Instruments Shop for their support of the high precision maching and Dr. P. Siegel and Dr. J. Pearson for many helpful discussions.

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