A Single-Waveguide In-Phase Power-Combined Frequency Doubler at 190 GHz

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Abstract—This work represents the first demonstration of in-phase power-combined frequency multipliers above 100 GHz based on a dual-chip single-waveguide topology, which consists of two integrated circuits symmetrically placed along the E-plane of a single transmission waveguide. This strategy increases by a factor of 2 the maximum sustainable input power with regard to traditional waveguide multipliers. A biasless 190 GHz Schottky doubler based on this novel concept has been designed and tested with a 6–10% conversion efficiency measured across a 177–202 GHz band when driven with a 50–100 mW input power at 300 K.

Index Terms—Frequency multiplier, local oscillator, planar Schottky diode, power-combining, submillimeter wavelengths.

I. INTRODUCTION

FOR the last two decades, GaAs Schottky diode based multiplied local oscillator (LO) sources have been the preferred devices to up-convert the signal from the available 100–150 mW solid-state sources at W-band up to terahertz frequencies [1], [2]. The conversion efficiency of current Schottky multipliers at 300 K ranges from $\sim 30\%$ (doublers) and $\sim 16\%$ (triplers) @ 200 GHz to $\sim 2.5\%$ @ 900 GHz and $\sim 1\%$ @ 1.9 THz (1–3 μW output power) [1]–[3]. Other devices such as Heterostructure Barrier Varactors (HBV) are suited for odd-order multipliers and have reached 11% efficiency at 250 GHz [4]. The recent progress in power-combined MMIC amplifiers based on GaN transistors, providing up to 5 W at W-band [5], makes it possible now to develop space-qualified
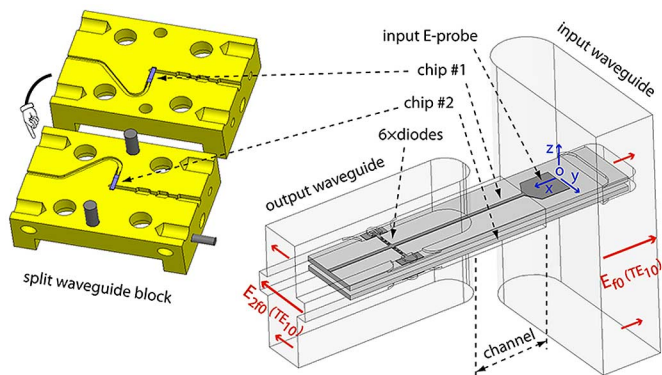
Fig. 1. Dual-chip single-waveguide power-combined scheme for multipliers.

all solid-state sources and detectors beyond 2 THz with Schottky technology [3]. Nevertheless, a direct adaptation of the available designs to higher input powers, by increasing either the device area or the number of diodes within the chip, is not possible due to the circuit size limit imposed by the height of the transmission waveguide and other constraints, so novel technological solutions are necessary [6]. The use of wide bandgap semiconductors such as *GaN* for the first multiplication stages may increase the power-handling capabilities of Schottky diodes almost an order of magnitude with similar anode areas [7]. The number of diodes can also be augmented by a factor of 2 by power combining identical multipliers using compact Y-junctions or hybrid couplers without affecting the efficiency with regard to single-chip multipliers [3], [6]. Moreover, quasi-optical power combining has been successfully employed to combine the outputs of HBV arrays [8]. Lastly, substrates with high-thermal conductivity such as diamond can greatly reduce the multiplier temperature and the risk of burnout problems in high power multipliers [9].

In this context, the topology shown in Fig. 1 represents a further step in power-combined multipliers by adding an extra symmetry plane to the circuit that allows twice the number of diodes to be included. It features two MMIC chips symmetrically placed along the E-plane within a unique transmission waveguide (dual-chip single-waveguide scheme). This strategy could double the power-handling capabilities of multipliers without the necessity of duplicating the input and output matching networks, unlike in [3], [6]. In this work, a broadband 190 GHz doubler has been successfully designed and tested using the standard BES Schottky diode process of UMS. Since the diodes provided by UMS were not optimized for multiplier operation, the final goal has not been to achieve state-of-the-art efficiency but to prove the viability of the concept. The work herein shows an excellent agreement between theory and measurements and represents the first demonstration above
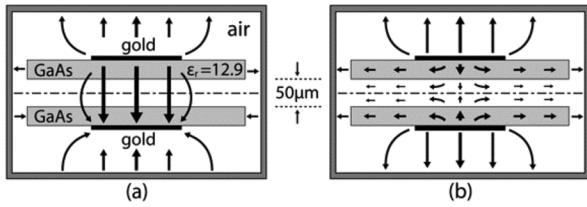
Fig. 2. Quasi-TEM modes along the H-plane of the rectangular waveguide: (a) Perfect Electric Conductor plane of symmetry and (b) Perfect Magnetic Conductor plane of symmetry. At E-probes, field lines of the exciting TE_{10} mode acquire the symmetry of (b). Hence, only this quasi-TEM mode is coupled. Field lines are at the OYZ cross-section indicated in Fig. 1.
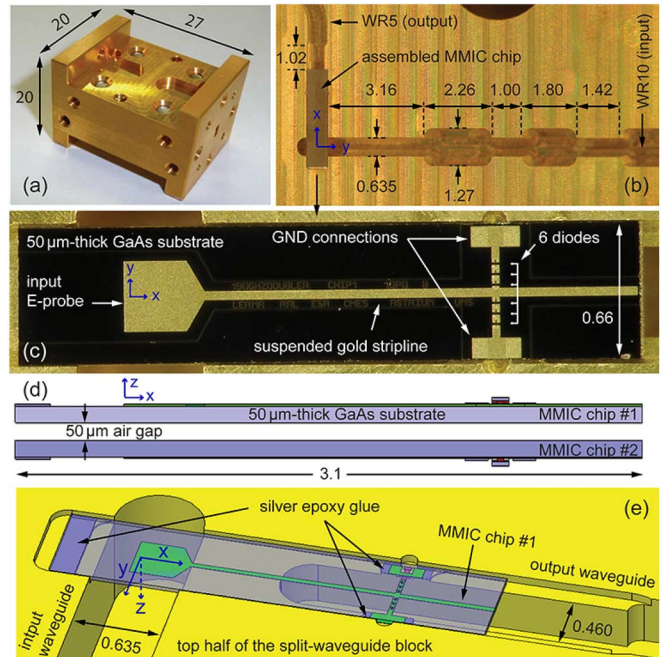

Fig. 3. (a) Machined split-block. (b) Close-up photograph of the top half of the split-block showing input and output matching steps. (c) Multiplier chip layout. (d) Diagram showing the position of the two chips after assembly, (e) and the assembly of each individual chip on each half of the block. Dimensions are in millimeters if not otherwise specified.

100 GHz of this novel dual-chip power-combining scheme. The measured efficiency is similar to that achieved with an equivalent single-chip 190 GHz doubler presented in [10].

II. Single-Waveguide Power-Combined Scheme

The multiplier uses a split-waveguide block design (see Figs. 1 and 3) with two MMIC chips inserted within the same transmission waveguide close to its center, where the electric field of the TE_{10} mode is maximum. Note that this topology is electrically and thermally identical to an equivalent single-chip multiplier driven with half the LO power. At the input waveguide, each E-plane probe couples one half of the exciting signal to each MMIC chip. Two quasi-TEM modes, illustrated in Fig. 2, might propagate the input signal through the suspended striplines towards the diodes located at the output waveguide. However, at the E-probes, only the field lines of the quasi-TEM mode in Fig. 2(b) have the appropriate symmetry to be excited by the input TE_{10} mode. Whenever the circuit symmetry is preserved during fabrication and installation, this enables the possibility to define a perfect magnetic-wall boundary at the symmetry plane and simulate only half the structure (one chip), reducing considerably the design complexity. The nonlinear capacitance of the diodes generates the second harmonic of the input frequency, which excites the TE_{10} mode in the output waveguide. The reduced waveguide channel (210 μm$\times$ 710 μm) between the input and output waveguide acts as a filter that prevents the output TE_{10} mode from leaking into the input waveguide. The circuit is completed with a succession of waveguide sections of different heights and lengths to provide broadband input and output matching, as detailed in Fig. 3(b). Each MMIC chip features 6 diodes (12 diodes in total) of about 14 μm^2 in a balanced configuration at RF, connected in series at dc, and monolithically integrated on a 50 μm-thick GaAs substrate, as shown in Fig. 3(c). The epilayer doping is approximately $1 \cdot 10^{17}$ cm^{-3}.

III. Circuit Design and Fabrication

The design was driven by the necessity to minimize the impact of possible imprecision in the control of the distance that separates the two MMIC chips [see Figs. 1 and 3(d)]. This gap needs to be constant along all the chip size in order not to break the circuit symmetry, which would result in a dramatic degradation of the multiplier performance, as discussed in detail in [11]. The shorter the distance, the better input coupling but the more difficult to assemble the chips with the correct separation. Hence, a metal-to-metal trade-off distance of 150 μm has been selected to guarantee a precise assembly, as illustrated

in Fig. 3(d). The use of robust 50 μm-thick rectangular substrates, together with a simple fabrication process involving only dicing and lapping, avoids bending problems during assembly that would break the symmetry [11] and guarantees an adequate heat transfer from the diodes to the block, which is critical at higher power levels.

The design methodology combines Agilent ADS linear/nonlinear harmonic balance circuit simulation to optimize the performance of the circuit, with Ansoft HFSS 3-D EM simulation to accurately model the diode geometry and waveguide structure, as in [6]. Since UMS-BES Schottky process is aimed for frequency mixers, the characteristics of the available diodes were not adequate to achieve state-of-the art multiplier performance. The diodes feature very short epilayers (100 nm) and subsequently low breakdown voltages ($V_{br,\min} = -5$ V). Hence, a biasless design was chosen to guarantee a safe operation regime for the multiplier. In addition, the epilayer is already fully depleted at 0 volts, resulting in a nearly flat voltage-capacitance (C-V) characteristics for reverse voltages. The subsequent loss in capacitance nonlinearity compromises the attainable efficiency. Under these conditions, only 10% peak efficiency was expected for the design despite that a 25% efficiency could be achieved with this topology with more suitable diodes without the limitation imposed by the short epilayers [11]. A detailed study on the optimum characteristics of Schottky multipliers above 100 GHz can be found in [12].

The nonlinear diode model of ADS cannot well represent these particular operating conditions because it does not include the impact of the epilayer thickness. Hence, we have developed a custom symbolic defined device (SDD) model in ADS to accurately model the actual response of UMS-BES Schottky diodes.

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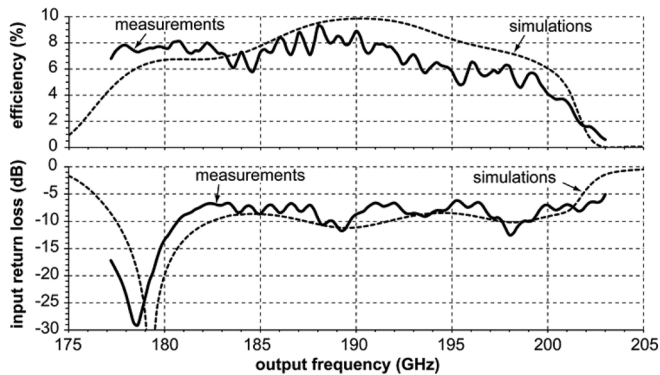

Fig. 4. Simulated and measured efficiency (top) and input return loss (bottom) of the 190 GHz dual-chip frequency doubler with 80 mW of input power.

The model represents the diode by means of its equivalent circuit: A nonlinear capacitance in parallel with a current generator, and in series with the series resistance. Fitted equations for the C-V characteristics were directly provided by UMS, and the current-voltage (I-V) characteristics have been derived from on-chip dc measurements performed at the Observatory of Paris. The actual dc series resistance of the diodes ($R_s = 4.4\,\Omega$) have been extracted from I-V curves measured under high forward bias currents to ensure flat-band operation of the diodes (i.e., zero junction resistance). A number of tests of various diodes have been performed to eliminate the impact of the probes resistance on the results. As will be shown later, the predicted performance with this model is in excellent agreement with RF measurement.

The doubler split-block, shown in Fig. 3(a), was machined at the Rutherford Appleton Lab., UK. As expected, the assembly was very simple and repeatable, and it was not difficult to well align the chips preserving the circuit symmetry. Each chip is fixed face-down with silver epoxy glue to one half of the block (ground connection) as depicted in Figs. 1 and 3(e).

IV. MULTIPLIER MEASUREMENTS

The source used to test the doubler consisted of a synthesizer tuned in the 29.5–33.83 GHz band followed by an active tripler, a WR10 isolator, one of two different power amplifiers to cover either the 88–94 GHz or the 94–102 GHz band, another WR10 isolator and a high-precision attenuator to ensure a constant input power across the measured frequency bandwidth. The input power of the doubler was directly controlled by the attenuator and monitored using an Erickson Instruments PM2 power meter[1]. The calibration of the input power was made separately using this calorimeter. The output power of the doubler was measured using the same Erickson PM2 power meter together with a 1.5 in long WR10 to WR5 waveguide transition (the measured output power has not been corrected for the transition loss). For the input return loss measurement, a 10 dB directional coupler was placed between the attenuator and the frequency doubler. The reflected input power was measured by means of an Agilent WR10 W8486A power sensor and an Agilent N1912A power meter[2].

A 9% peak efficiency and a $\sim 12\%$ 3 dB bandwidth have been measured for the dual-chip single-waveguide 190 GHz doubler

[1]Virginia Diodes Inc, 979 2nd Street SE, Charlottesville, VA.

[2]Agilent Technologies, Inc., 5301 Stevens Creek Blvd., Santa Clara, CA.

when pumped with a 80 mW constant input power across the measured frequency band (see Fig. 4). Power sweeps between 20 mW and 120 mW input power have also been performed with measured peak efficiencies of 10.2% @ 120 mW, 10.0% @ 100 mW, 9.0% @ 80 mW, 8.1% @ 63 mW, 6.7% @ 50 mW and 4.3% @ 25 mW. A comparison between measurements and simulation results is provided in Fig. 4. The very good agreement for both conversion efficiency and input return loss proves the validity of the employed design method and demonstrates the feasibility of the proposed single-waveguide in-phase power-combining scheme. It must be emphasized that the single-waveguide dual-chip doubler demonstrated herein is compact, fixed-tuned and biasless.

V. CONCLUSION

A single-waveguide in-phase power-combined 190 GHz biasless frequency doubler featuring two identical MMIC multiplier chips within the same transmission waveguide has been designed and tested. The achieved doubler performance with the available mixer-optimized UMS diodes is well suited for medium power sources used in test equipment where the ultimate performance is not necessary. Nevertheless, state-of-the-art efficiencies could be obtained with this scheme by using biased Schottky diodes properly optimized for multiplier operation. This work represents the first demonstration of this novel circuit topology that increases by a factor of 2 the power handling capabilities of traditional multipliers. This scheme is simple and reproducible, and we believe that it could be widely employed in the short term to take advantage of the increasing LO power at W-band in order to extend the use of solid-state multiplied LO chains beyond 2 THz. It could also be potentially applied to power amplifiers.

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