Design of a Wideband 900 GHz Balanced Frequency Tripler for Radioastronomy

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Abstract

We report on the design of a fix-tuned split-block waveguide balanced frequency tripler working nominally at 900 GHz. It uses a GaAs Schottky planar diode pair in a balanced configuration. The circuit will be fabricated with JPL membrane technology in order to minimize dielectric loading. The multiplier is bias-less to dramatically ease the mounting and the operating procedure. At room temperature, the expected output power is 50-130 µW in the band 800-970 GHz when the tripler is pumped with 4 mW. By modifying the waveguide input and output matching circuit, the multiplier can be tuned to operate at lower frequencies.

Introduction

The current importance of astrophysics related, high-resolution spectroscopy in the submillimeter range is highlighted by the current build-up of the Heterodyne Instrument for the Far Infrared (HIFI) on the European Space Agency's Herschel Space Observatory and the Atacama Large Millimeter Array (ALMA). HIFI and ALMA will employ high frequency, high sensitivity heterodyne receivers to discover, measure and map atomic and molecular gases in and around star forming regions, nebulae and galaxies. A critical component of each receiver is the local oscillator (LO) source. Sources in the sub-millimeter range have been historically extremely difficult to build and deploy. They used to employ whisker contacted Schottky diode multipliers, which require tedious assembly processes. Since the mid 90's, planar Schottky diodes have revolutionized the field of multiplied sources [1],[2], and in the last few years decisive progress has been made towards implementing practical planar Schottky diode varactors in the sub-millimeter and THz range [3],[4],[5],[6]. In this context, we present the design of a wide-band fix-tuned 900 GHz waveguide tripler optimized for medium-low input power. The circuit has been made bias-less to greatly ease the assembly process, to make the multiplier ESD-safe and to simplify the operating procedure of the 900 GHz local oscillator chain.

Balanced design

When designing a frequency tripler, the matching at the second harmonic is particularly critical: the impedance at the second harmonic should be as close as possible to a pure reactance. The best way to meet this requirement is to balance the circuit and to trap the second harmonic in a virtual loop.

In our design, this loops is created by two diodes that are in series at DC but appear to be in an anti-parallel configuration at the RF, due to the symmetry of the excitation and the symmetry of the circuit. This virtual loop can only work if the suspended micro-strip line,with which the diodes are connected to cannot propagate the parasitic (TE) mode at the second harmonic. Figure 1 shows a block diagram of the triplers: an E-plane probe located in the input rectangular-waveguide couples the signal at the fundamental frequency to the suspended microstrip line. The diodes are connected to an E-plane probe that couples the third harmonic to the output waveguide.

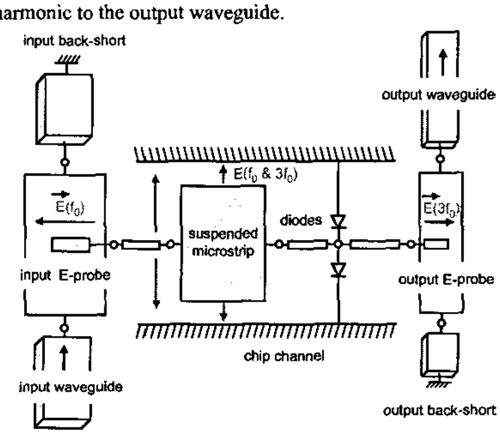

Fig. 1: Block diagram of the 900 GHz balanced tripler.

The matching of the diode is performed both by a succession of high and low impedance sections printed on chip and by the input and the output probes with their respective back-shorts. To widen the bandwidth, the circuit may feature additional matching elements in the input and output waveguides, made with a succession of waveguide sections of different heights and lengths. The optimization methodology was described in [5]. It requires intensive 3D electromagnetic simulations that were performed with the finite element method. The non-linear response of the circuit is given by a harmonic balance code. The Schottky diode is described by a simplified model based on [1]. The junction capacitances are calculated with an external program that takes into account the fringing fields.

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Topology and expected performances

The multiplier is a split-block waveguide tripler similar to a higher frequency tripler designed for HIFI [5],[6]. The active devices as well as part of the matching circuit are implanted on a 3 μm-thick GaAs membrane. The same design can also work on a 5 μm-thick membrane with little degradation in the performances.

The rectangular anodes are nominally 0.4 μm wide and 1.1 μm long; doping is 5E17 cm^{-3}; corresponding zero-bias junction capacitance and expected series resistance per diode are respectively 1.3 fF and 40 Ω. Figure 2 shows a 3D view of the 900 GHz tripler. Due to the absence of a bias circuit, the assembly of the multiplier is particularly straight-forward.

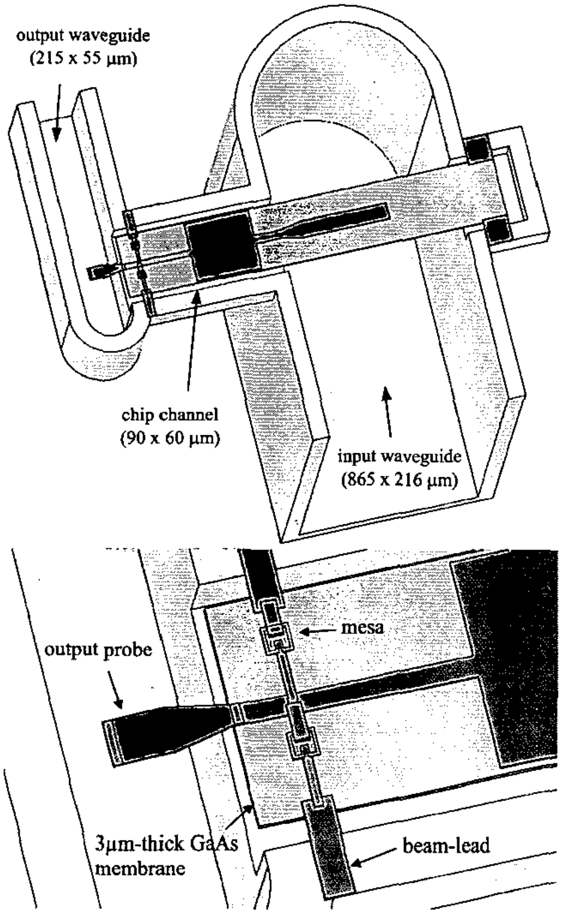

Fig. 2: 3D view of the 900 GHz balanced tripler. Bottom view details the diode area.

Figure 3 shows the expected output power and input coupling for 4 mW of input power in the 800-1000 GHz band. A bias-able version of this design is under study. Output power could be greatly enhanced (by a factor of two approximately) due to the possibility of reverse-biasing the diodes and subsequently reducing the forward current through them. To take full advantage of a bias-able circuit, the anodes have to be made bigger.

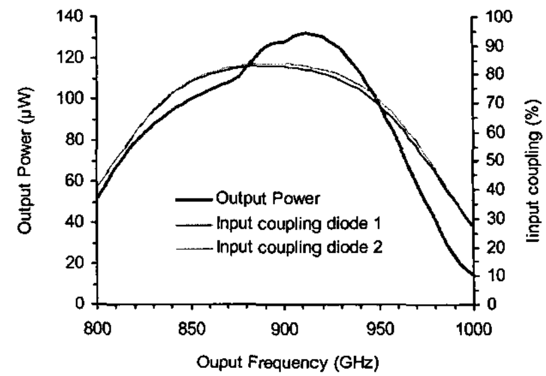

Fig. 3: Simulated output power and input coupling as a function of frequency with 4 mW of input power. The circuit is fix-tuned and bias-less. The input coupling reaches 80% for both diodes. By adding steps in the input waveguide, it can be made flatter.

Conclusion

An easy to assemble and operate 900 GHz tripler has been designed. The circuit should be able to cover about 20% bandwidth with enough power to pump SIS mixers working in the 800-1000 GHz band. With the same chips, by modifying the waveguide matching circuit, lower frequency operations can also be achieved.

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