

Design Considerations for a 1.9 THz Frequency Tripler Based on Membrane Technology

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Abstract — The design of membrane-based Schottky planar diode frequency triplers to 1.9 THz is discussed. Both, balanced and unbalanced circuit designs are proposed and compared. The simulations show that with 2.5 to 3.5 mW of input power the balanced triplers can produce sufficient power to pump hot electron bolometer mixers. However, if the available input power is limited to 1 mW then the unbalanced design can outperform the balanced design. Both designs are currently being fabricated and will be tested in the near future.

I. INTRODUCTION

In the last few years tremendous progress has been made towards implementing practical planar Schottky diode varactors in the THz range [1-4]. The present paper deals with the design of a 1.9 THz frequency tripler that can be used as the last stage of a multiple stage local oscillator (LO) chain to pump hot electron bolometer (HEB) mixers for heterodyne receivers dedicated to radio astronomy.

Implementation at these frequencies can be achieved with a number of cascaded multiplier stages driven by a HEMT based power amplifier module. Starting with power amplifier modules in the 71-79 GHz range one can implement a $\times 2 \times 2 \times 2 \times 3$ chain to provide the LO source. It is also possible to use amplifier modules in the range of 90-110 GHz with a $\times 2 \times 3 \times 3$ multiplier chain. This paper will address the methodology in-

involved in designing the 1.9 THz tripler based on the membrane multiplier technology that has been demonstrated successfully to 1200 GHz [2,3].

II. DESIGN METHODOLOGY

A common method employed to design and optimize diode multiplier circuits is to first optimize the diode parameters using non-linear codes (such as harmonic balance). The diode impedance is then properly matched to the input and output circuits utilizing linear circuit synthesis. This approach is relatively fast and has shown to work very well with balanced doublers in the sub-THz range [1,4], since the input and output circuits can be optimized independently. However, in our approach we have exclusively used non-linear codes to simultaneously optimize the input, output and the idler frequency for designing of the triplers to 1.9 THz. Though, this places further burden on the computational hardware, it allows one to simultaneously optimize the diode physical structure along with the embedding circuitry for maximum advantage.

Diode model: A complete and accurate physical diode model that can predict device response at these frequencies is still not available. A practical approach is to use a simple model of the diode that can easily be described in commercial codes including significant efficiency limiting phenomena

such as breakdown voltage and current saturation. Such an exercise has been carried out in [5] for doublers assuming very limited input power (0.1 mW). Based on this exercise doublers in the 1.9 THz range at room temperature should be designed according to:

$$R_s \times C_j(0) = 120 \Omega \cdot \text{fF} \quad (1)$$

Where, R_s is the series resistance and $C_j(0)$ is the zero bias junction capacitance.

For the 1.9 THz tripler a zero bias junction capacitance of 0.6 to 1 fF is assumed based on the wafer doping ($5E17 \text{ cm}^{-3}$) and reasonable minimum dimensions consistent with the membrane fabrication process. Furthermore, the model was modified by introducing a linear frequency dependence of the RF series resistance. The series resistances of the 1.9 THz tripler was chosen by extrapolating linearly the series resistances used to model an existing (and characterized) 1.2 THz balanced tripler [4] in accordance with (1).

Operating temperature: The multiplier is designed for an operating temperature of 300 K, although there are several applications where these multipliers will have to be cooled to around 100 K. The multiplier chains are expected to deliver more power when cooled [6,7].

Losses: At 1.9THz, losses in the circuitry are a major concern. Losses not only introduce a linear attenuation of the signals. In a multiplier circuit, losses can also make the matching of the diode very inefficient. Simulations show that a diode with $C_j(0)=1\text{fF}$, pumped with 2.5mW at 633GHz, can transfer power to the third harmonic at 1.9 THz up to thirty times more efficiently when matched by an optimal and ideal circuit, than when matched by a circuit feasible with the state-of-the-art technology (with an

ideal matching circuit the diode works in a true varactor mode, with a feasible matching circuit the same diode works mostly in a varistor mode). The losses must be included during the optimization of the circuit and not after¹. Matching circuits designed with no loss could be in practice “surprisingly” lossy and not fully optimum.

Topology limitation & accuracy: Another major difficulty encountered in the design of terahertz multipliers is the limitation in the topology of the circuits. This limitation is mainly due to the RF losses that the metallic parts of the circuits can induce. Actually, to keep the losses acceptable, it is necessary to use matching elements made of sections of waveguides in which the currents flow with a low surface density. The rectangular waveguide, the coaxial waveguide or the suspended microstrip are usually good candidates for such a requirement. Unfortunately the topology of the circuits feasible with such waveguides is pretty limited. In addition, the active devices are totally immersed in these waveguides, a fact that does not facilitate efficient modeling.

The accuracy of the fabricated circuits is also a concern when working at these frequencies. It is important to design the circuits to be as tolerant as possible to fabrication and assembly variations. To allow for machining tolerances in the waveguide blocks it is recommended to integrate on chip the critical matching elements in order to take advantage of the tighter tolerances associated with micro-photolithographic techniques. Circuits fabricated on thin dielectric membranes combine low loss and accuracy providing for a more stable and robust implementation.

¹ Depending on the method used to simulate the different portions of the circuit, tacking into account the losses can lead to long simulation times. The temptation is to simulate the structure with no loss for the optimization and to check the final circuit including the losses.

The tools: HP ADS (Advanced Design System) was used for the non-linear simulations and optimizations. The 3-D electromagnetic solver, HFSS (High Frequency Structure Simulator) was used for the extraction of the S-parameters of each part of the circuit.

III. TO BALANCE OR NOT TO BALANCE THE CIRCUIT

Balance doublers and triplers at lower frequencies have demonstrated remarkable performance to date. However, at 1.9 THz it is not obvious, first of all, if balanced circuits can be built, and secondly if they would be preferable.

Besides the several constraints represented in the previous section another practical constraint that must be acknowledged for any high frequency multiplier design is the fact that only limited amount of RF power will be available to drive the multiplier. When the pump power of a multiplier is small, the diode cannot be properly modulated. At the limit, the power conversion from the fundamental to the n^{th} harmonic follows a law that asymptotically tends to :

$$P_n \xrightarrow{P_1 \rightarrow 0} \alpha(f) \times P_1^n \quad (2)$$

or in the logarithmic form :

$$\text{Log}(P_n) \xrightarrow{P_1 \rightarrow 0} \alpha'(f) + n \times \text{Log}(P_1) \quad (3)$$

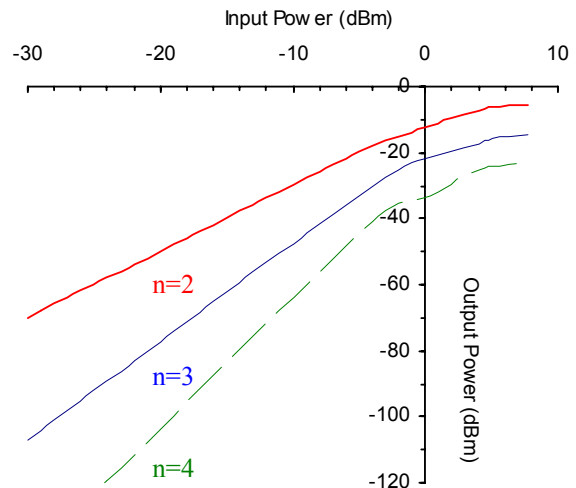
where P_n is the power produced at n^{th} harmonic, P_1 is the pump power, $\alpha(f)$ is a coefficient that depends on the diode and the frequency (Figure 1). Equation (2) shows that for a tripler ($n=3$), dividing the pump power by two can divide the output power delivered by the diode by eight (and the conversion efficiency by four).

When one has to choose between designing a balanced multiplier that requires at least two diodes, or an unbalanced multiplier that requires only one, the relation between the

pump power and the efficiency of a diode has to be taken into account. The single diode of an unbalanced multiplier will receive twice the power that each diode of the simplest balanced multiplier will receive. In addition, the higher the order of multiplication, the bigger the difference in the conversion efficiency of the diode. On one hand, balancing a multiplier considerably simplifies the matching circuit. In addition, there is the possibility to reduce the size of the anode to compensate the decrease of pump power (a smaller diode will be easier to modulate than a bigger one). In practice, this possibility is limited at high frequencies by the fact that a smaller anode presents a higher series resistance, and also by the fact that there is a minimum size for the anode.

Thus, for the 1900 GHz tripler both a balanced and an unbalanced approach was attempted.

Fig. 1 The calculated output power versus input



power of an ideal frequency doubler (top), tripler (middle) and quadrupler (bottom) fits equation (3). The multipliers are optimized for an input frequency of 500GHz and an input power of 3.5mW. The diode is the same for all the multipliers — $C_j(0)=1\text{fF}$, bias fixed to zero volts.

IV. A FAMILY OF TRIPLERS FOR 1.3 THZ TO 1.9 THZ

We designed a series of both single-diode and balanced frequency triplers for the range of frequencies 1300-1900 GHz though only the 1.9 THz tripler will be discussed in the present paper. All of them utilize the technology involved in the very successful 1.2 THz tripler [8]. The diode, as well as the circuit, is fabricated on a GaAs substrate, which, once etched, becomes a three-micron thick membrane. The circuit is mounted in a gold-plated waveguide structure split into two precision-machined halves. The membrane is held in the middle of the waveguide structure by one-micron-thick gold beam-leads. There is no frame to support the membrane. Although such a thin circuit may look very fragile, it is surprisingly robust and can be handled without causing damage.

Topology: Both circuits have the same basic topology as shown in Figure 2. An E-plane probe located in the input waveguide couples the signal at the fundamental frequency to a suspended microstrip waveguide that can propagate only the TEM mode. In order to keep this waveguide single-moded, the dimensions of the channel in which the membrane is inserted have to be chosen with care. The cross-section of the channel is only 25 to 64 micron wide by 25 micron high. The diode(s) is (are) placed as close as possible to the output waveguide (8 to 10 microns). It (they) is (are) connected to an E-field probe that couples the third harmonic to the output waveguide (the second harmonic is kept below cutoff). The matching of the diode is performed both by a succession of high and low impedance sections fabricated on chip and by the input and the output probes, with their respective backshorts and waveguide steps. The difference between the two triplers comes mainly from the diode implementation as shown in Figure 3.

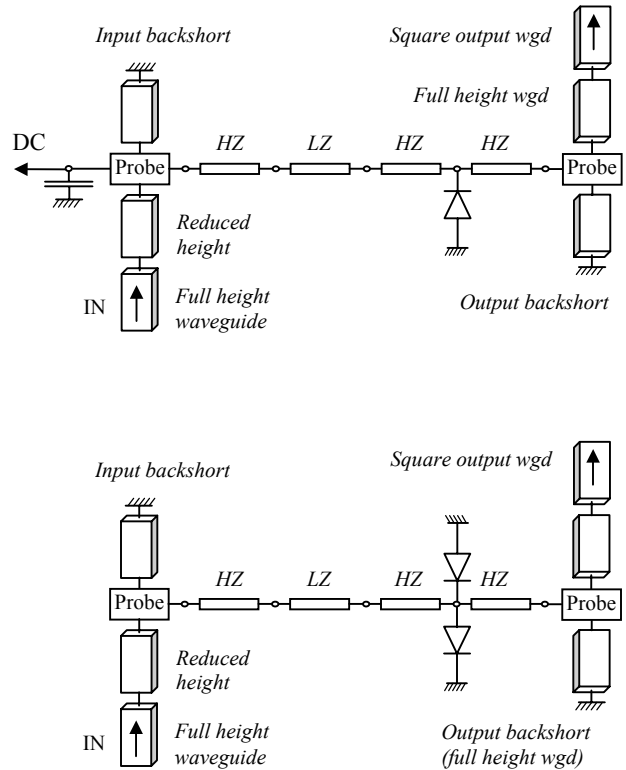


Fig. 2: Electrical schematic representation of the unbalanced (top) and balanced (bottom) triplers at 1.9 THz (HZ stands for high impedance line, LZ stands for low impedance line).

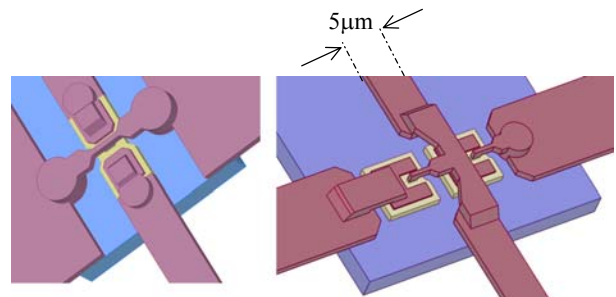


Fig. 3: Detail of the diode area for the unbalanced (left) and balanced (right) triplers.

The anode of the unbalanced design has a very small mesa (4x9 microns) with a sym-

metrical anode that is grounded on both sides of the channel by two beam-leads. Each side of the mesa is connected to a high impedance line. One of them continues to the output probe. This structure is very compact, but does result in an increase of the parasitic capacitance.

The balanced triplers have two anodes positioned on each side of the high impedance line. The diodes are connected in series at DC. One has its anode grounded at one side of the channel by a first beam-lead, the other has its cathode grounded to the other side of the channel by a second beam-lead. Due to the symmetry of the field at the fundamental frequency (TEM mode), the diodes appear in an anti-parallel configuration at RF. The second harmonic is trapped in a virtual loop [3] and cannot propagate in other parts of the circuit. This topology offers the advantage of a very small phase shift between the two anodes and the possibility to tune the matching at the idler frequency by adjusting the length of the beam-leads that ground the diodes. Thus, the length of the beam leads define the channel width. In addition, the size of the mesa is approaching a practical limit. To date mesa sizes of 10x10 micron have been implemented successfully with this technology. Pushing the size down to 7x7 microns increases the risk. At 1.9 THz, the width of the channel is 46x25 microns and the distance between the two mesas becomes small enough so that the high impedance line has to be partly placed on top of the mesa.

Bias scheme: At THz frequencies, the bias scheme is not a trivial problem. The unbalanced tripler can be biased through the input probe (that crosses the entire waveguide height) and the suspended microstrip line. A DC capacitor is implemented on chip to ground the RF signal. This solution can also work for the balanced designs but it is much

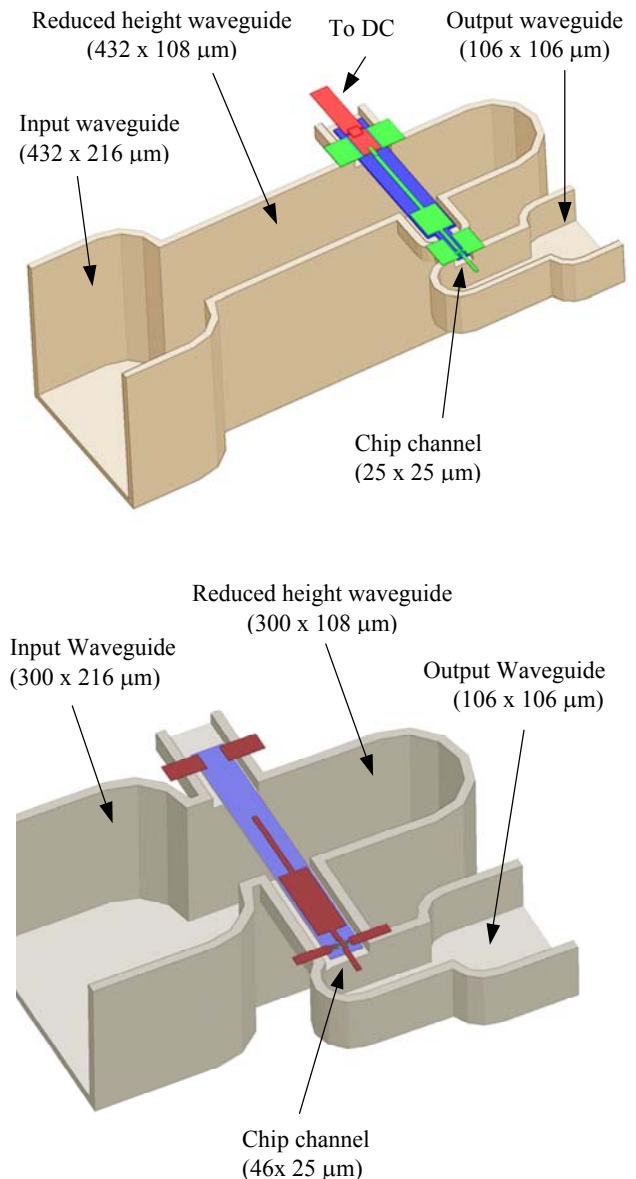


Fig. 4: 1.9THz unbalanced (top) & balanced triplers. The chips are held in the middle of the channel by one-micron thick beam-leads. The balanced circuit does not allow to bias the diodes.

more difficult to implement. Actually, two independent and opposite polarities have to be brought to the diodes. This can be done by inserting a small capacitor between the two mesas. The suspended microstrip must also be divided into two insulated lines. We found this solution feasible and useful for balanced triplers up to 1.6 THz. However, at

1.9 THz, due to the reduced dimensions, this is not practical. This limitation has an effect on the bandwidth of the tripler, but this effect is limited by the fact that the optimum bias of the diodes is close to zero volts. Figure 4 shows the implementation for each design.

Simulations: To complete the simulations a value for input power needs to be determined. An input power of 2.5mW at 633 GHz is assumed. This amount of power has not been demonstrated yet but certainly looks plausible given the recent results up to 400 GHz. Optimized simulations of both the balanced and unbalanced circuits are shown in Figure 5. The balanced configuration can provide twice as much power as the unbalanced design but only for a limited bandwidth. At the band edges both designs provide similar amounts of output power. The inability to further reduce the length of the beam-leads that ground the diodes of the balanced tripler is believed to be the main reason for this limitation.

We can compare the calculated performances of these multipliers with the performance of a diode that is matched by an ideal circuit. At 1.9 THz the difference between the designed circuit and the ideal circuit is shown in Figure 6. The balanced tripler design has one-eighth the efficiency as an ideal tripler using the same diode. Only 70% of the fundamental is coupled to the diodes. The low performance of this circuit is believed to be mainly due to a non-optimized idler forced by the current technology.

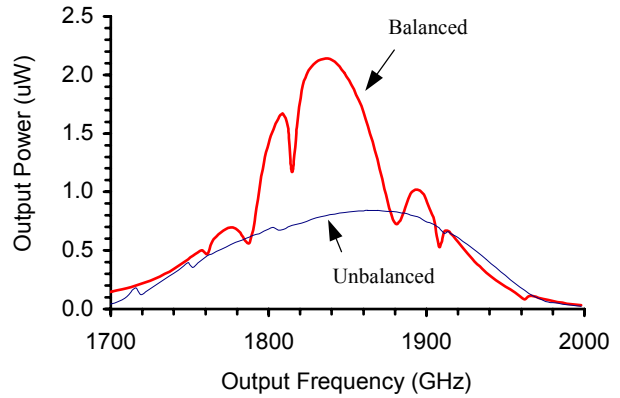


Fig. 5: Calculated output power of the 1.9 THz balanced and unbalanced triplers pumped with 2.5 mW. $C_j(0)=1\text{fF}$ for the unbalanced tripler, $C_j(0)=0.8\text{fF}$ for the balanced tripler.

An interesting simulation is to see what happens to the performance of the multipliers as input power is reduced. This is shown in Figure 7. As the input power drops below 1 mW the unbalanced circuit tends to outperform its balanced counterpart. One could argue that the designs have not been optimized for low power but in reality the anodes cannot be shrunk any more to offset the reduced input power level.

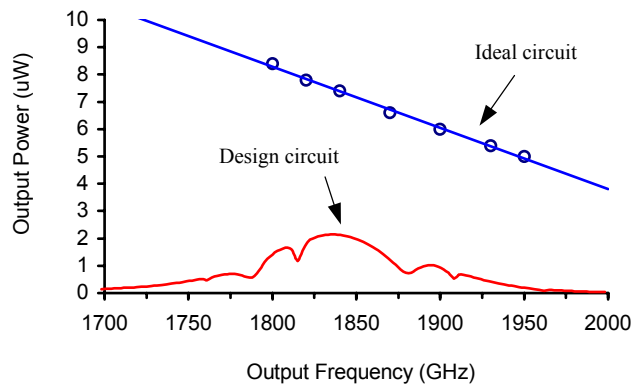


Fig. 6: Calculated output power of an ideal dual-diode 1.9 THz frequency tripler pumped with 2.5 mW (top) compared to the balanced circuit design (bottom). The diodes are the same in both case $C_j(0)=0.8\text{fF}$, same series resistance. The bias is fixed to zero volt in both cases.

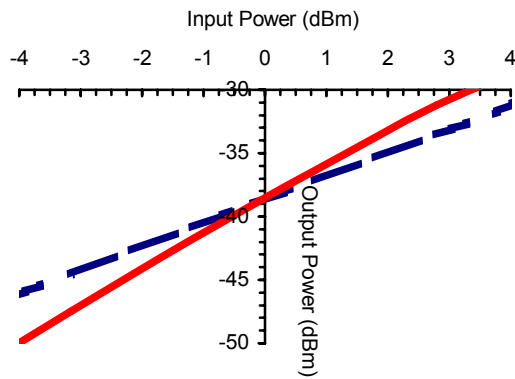


Fig. 7: Calculated output power of 1.9 THz frequency triplers versus input power. The unbalanced circuit (dashed line) performs better than the balanced circuit (solid line) when the input power falls below 1 mW.

V. CONCLUSION

Methodology for designing 1.9 THz planar triplers has been presented. This approach is intricately related to the current state-of-the-art fabrication technology. Both, balanced and unbalanced circuits have been simulated and compared. With sufficient input power the balanced approach is deemed preferable. Both chips are currently in fabrication and test results will be reported in the future.

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