Frequency Multipliers

Dr. Alain Maestrini

Université Pierre et Marie Curie-Paris 6, LISIF / Observatoire de Paris, LERMA

Formerly at Jet Propulsion Laboratory, California Institute of Technology

Acknowledgments

The Submillimeter-Wave Advanced Technology team,

Jet Propulsion Laboratory, California Institute of Technology

Peter Siegel, **Imran Mehdi**, John Ward, John Pearson, Hamid Javadi, Erich Schlecht, Goutam Chattopadhyay, Franck Maiwald, David Pukala

John Gill, JPL Micro Devices Laboratory

Peter Bruneau, James Crosby, JPL Space Instruments Shop

and

Neal Erickson, University of Massachusetts, Amherst, USA

Charlotte Tripon-Canseliet, Université Pierre et Marie Curie-Paris 6, LISIF

Outline

I. Introduction and fundamentals

- a) What is a frequency multiplier ?
- b) Why do we need them ?
- c) Noise issues
- d) What is the State-of-the-Art ?
- e) How does a frequency multiplier work?
- f) Devices for THz frequency multipliers

II. THz Frequency Multipliers

- a) Example 1 : 540-640GHz balanced tripler
- b) Design methods
- c) Example 2 : 1.9 THz balanced tripler

III. Perspective and Conclusions

- a) Power combining
- b) Integration

What is a Frequency Multiplier ?

Definition :

A frequency multiplier of order N is an electronic device that converts an input sinusoidal signal of frequency F_1 and power P_1 to an output sinusoidal signal of frequency $F_N=N\times F_1$ and power P_N .

In practice a frequency multiplier generates *unwanted harmonics* at frequencies $F_k=k\times F_1$ with $k\neq N$ and power P_k with

$$\sum_{k\neq 1, k\neq N}^{\infty} P_k \ll P_N$$

(frequency multiplier)

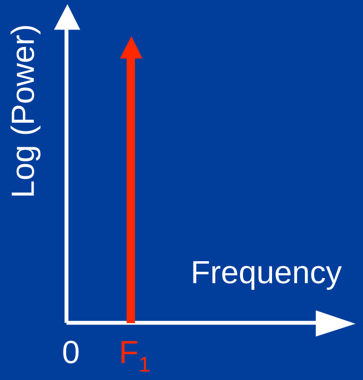
A frequency multiplier is therefore different from a *comb generator* that generates a series of harmonics which power decreases (usually) with the increasing frequency :

$$P_k \geq P_{k+1}$$

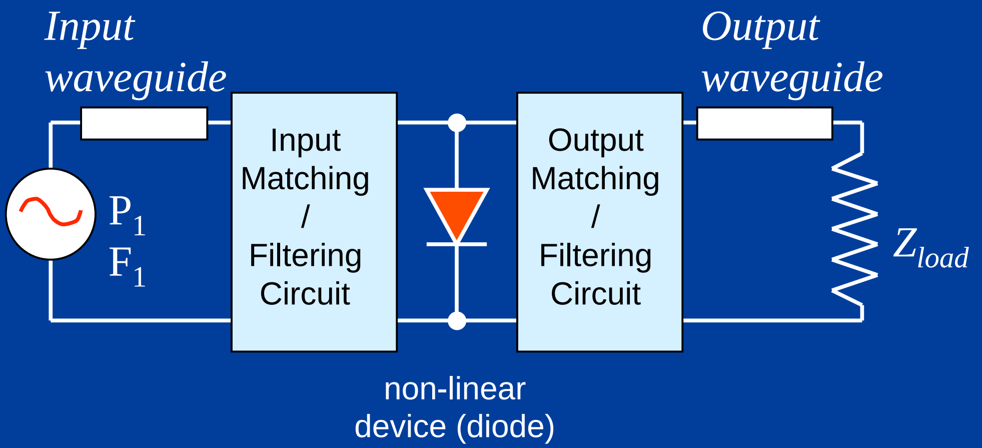
(comb generator)

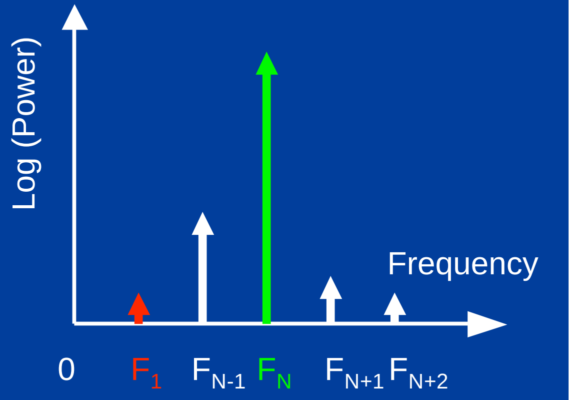
What is a Frequency Multiplier ?

Frequency Multiplier :



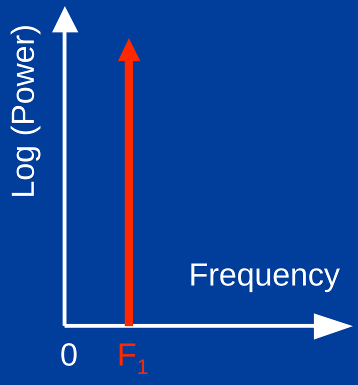
Spectrum of input signal



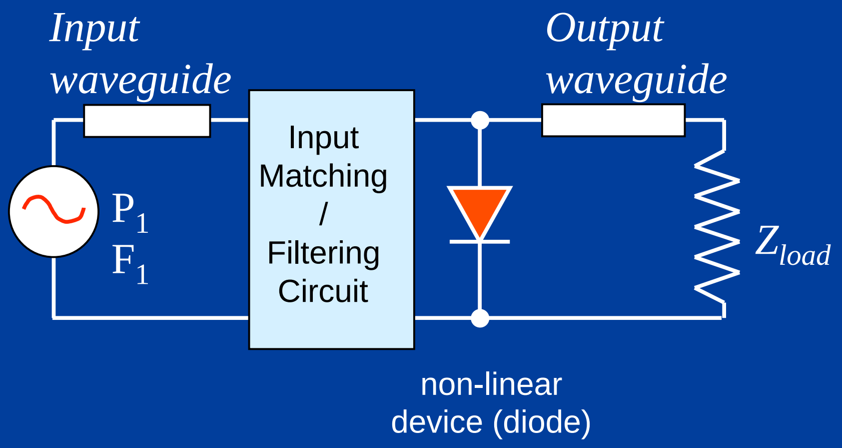


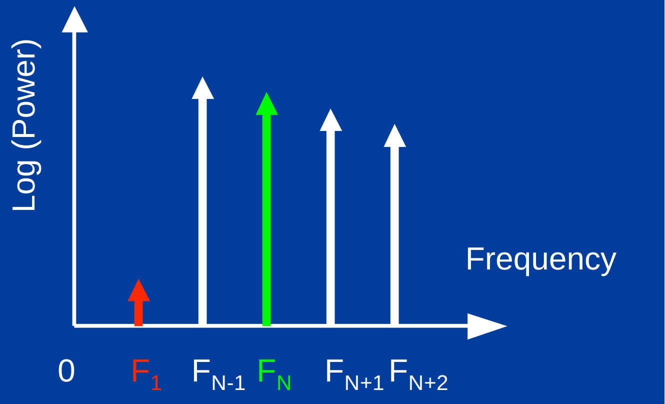
Spectrum of output signal

Comb Generator :



Spectrum of input signal





Spectrum of output signal

What is a Frequency Multiplier ?

Definition :

A frequency multiplier of order 2, 3, 4, N is called respectively a DOUBLER, a TRIPLER, a QUADRUPLER, a N-UPLER

Definition :

The conversion efficiency is the ratio $\eta=P_N/P_1$ (DC Power is not considered)

With 3-terminal devices (transistors) it is possible that $\eta \geq 1$. With 2-terminals devices (diodes) $\eta \leq 1$.

Maximum conversion efficiency of an ideal rectifier :

The conversion efficiency η of an ideal rectifier is limited by $1/N^2$ where N is the order of multiplication. Therefore, purely resistive non-linear devices are not suited for fabricating high-efficiency frequency multipliers.

What is a Frequency Multiplier ?

Maximum efficiency of an ideal reactive non-linear device :

The maximum conversion efficiency of an ideal reactive non-linear device (pure varactor, with no-loss) is η=1, regardless of the order of multiplication N (Penfield and Rafuse, 1962)

Practical frequency multipliers :

Series resistances in the device and circuit losses strongly affect the conversion efficiency. Reactive devices give more conversion efficiency than resistive devices but are harder to match other a wide frequency range (it is more difficult to couple the input signal to the device and more difficult to extract the output signal from the device).

High order frequency multipliers are very difficult to built. At frequencies above 100GHz, it is better to use a cascade of multipliers of lower order than a single high order multiplier.

What is a Frequency Multiplier ?

Conversion efficiency of a chain of multipliers :

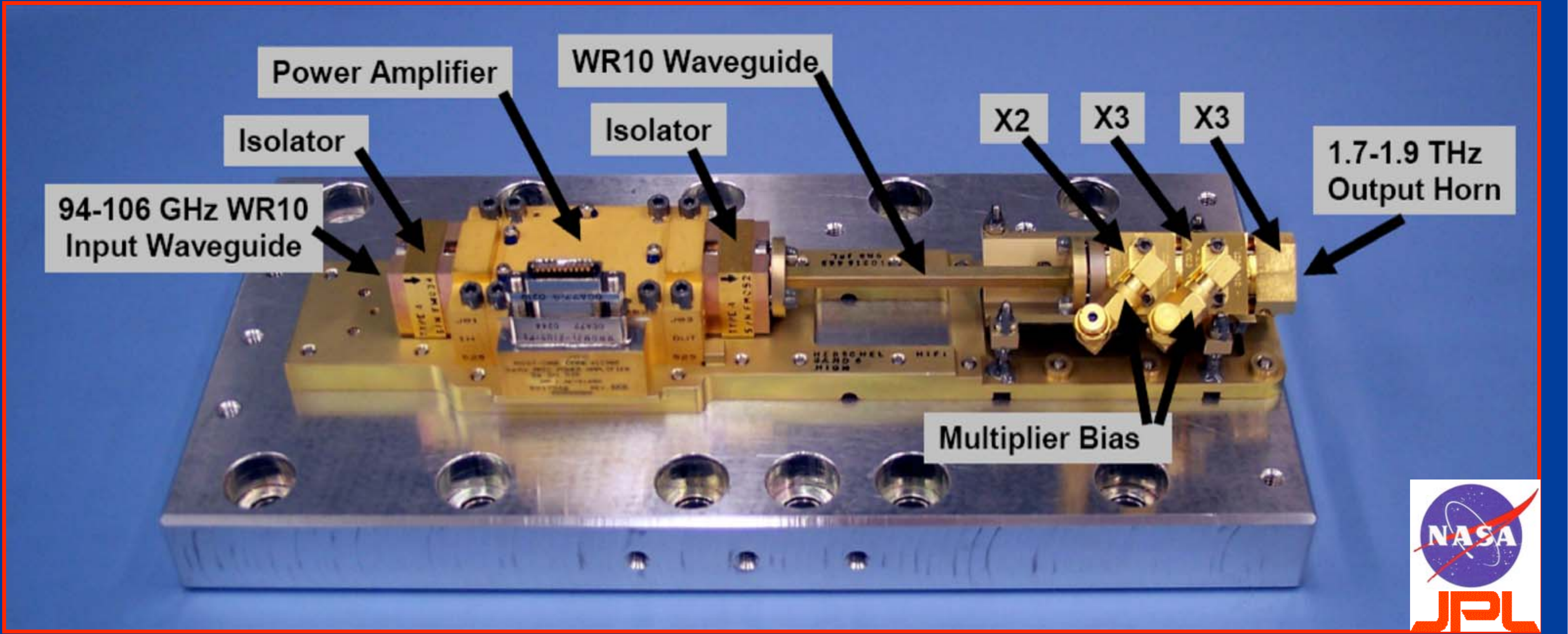
For a chain $\otimes N_1 \otimes N_2$ of two cascaded multipliers of respective order N_1 and N_2 , the conversion efficiency of the chain is $\eta[N_1,N_2]$.
A high order frequency multiplier of order $N_3=N_1 \times N_2$ has usually a conversion efficiency $\eta[N_3] < \eta[N_1,N_2]$.

The conversion efficiency of a multiplier depends on many parameters. At a given output frequency, order of multiplication and choice of device technology, the conversion efficiency depends on the input power. Consequently the efficiency of the chain $\otimes N_1 \otimes N_2$ is not necessary the same as the efficiency of the chain $\otimes N_2 \otimes N_1$:

$$\eta[N_1,N_2] \neq \eta[N_2,N_1]$$

It is common to write $\eta[N_1,N_2] = \eta[N_1] \times \eta[N_2]$ but this relation is valid only if the multipliers are *isolated* (no reflected power by the second multiplier at its input port can reach the first multiplier through its output port).

Example: 1.9THz Local Oscilator Chain for HIFI (HERSCHEL)



Why do we need frequency multipliers?

✓ Frequency multipliers are used to synthesize sinusoidal signals every time it is *easier / cheaper* to use a low frequency fundamental source cascaded with a frequency multiplier rather than using directly a fundamental source at the desired frequency.

Examples, frequency multipliers are used for:

- building ultra-stable sources at high frequencies using the reference signal given by a quartz / atomic clock
- generating signals where there is NO solid-state fundamental sources (filling the THz gap)

Noise issues

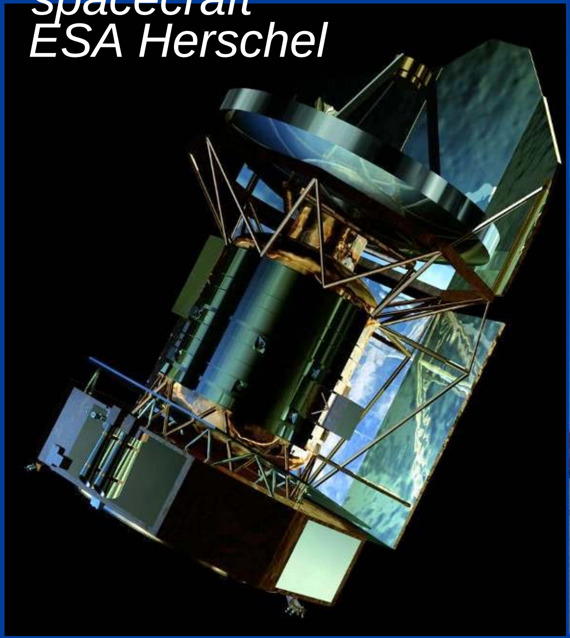
✓ A frequency multiplier degrades the phase-noise of the fundamental source by a factor ***20 log (N)*** , where N is the multiplication factor.

✓ A frequency multiplier adds amplitude modulation noise (AM), which power depends on the quality of the bias, the design and the fabrication of the circuit. In many cases AM noise is not significant compared to the additional phase noise introduced by frequency multiplication.

Sub-THz and THz Local Oscillators

NASA Aura spacecraft

ESA ROSETA

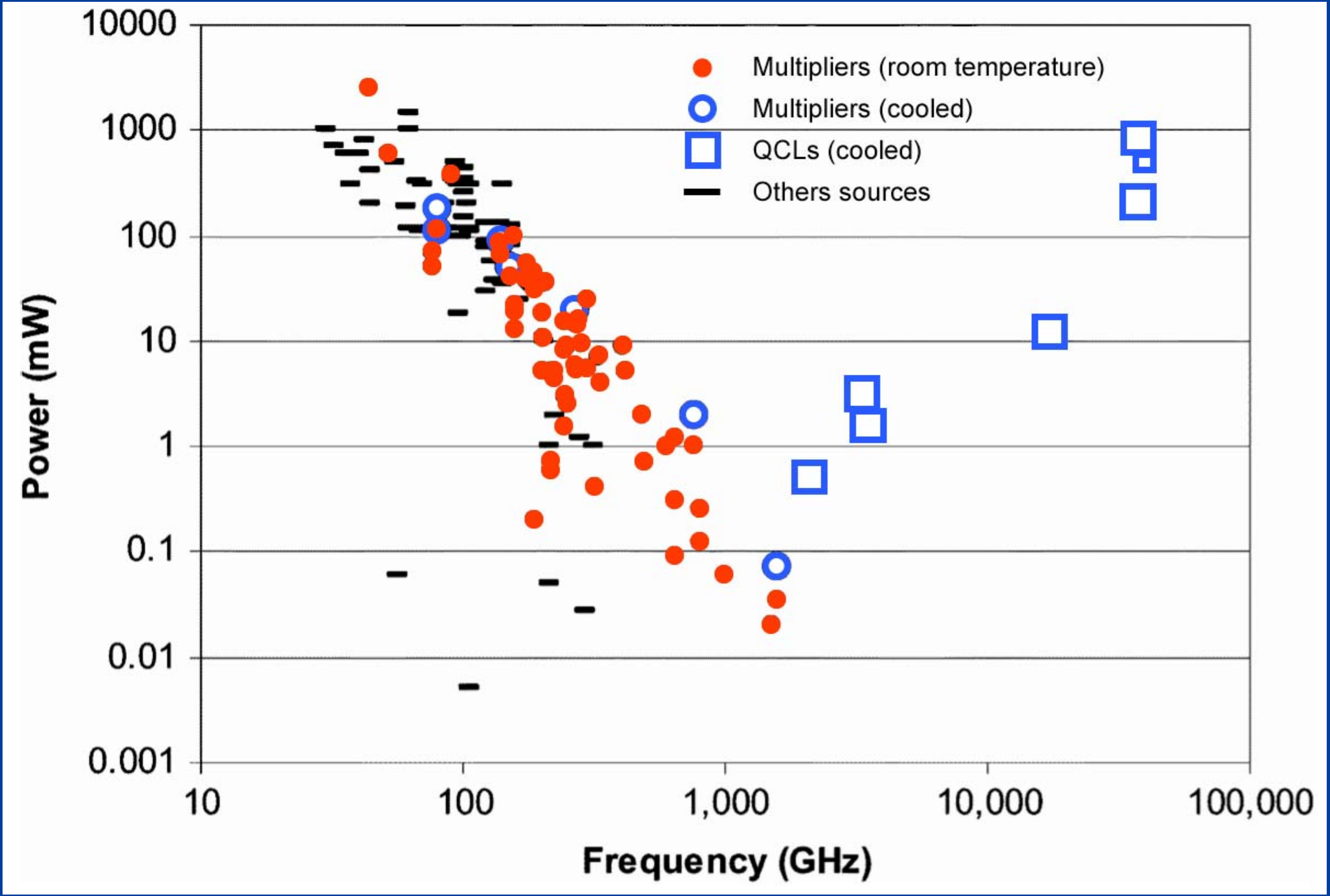


ESA Herschel

APEX / ALMA

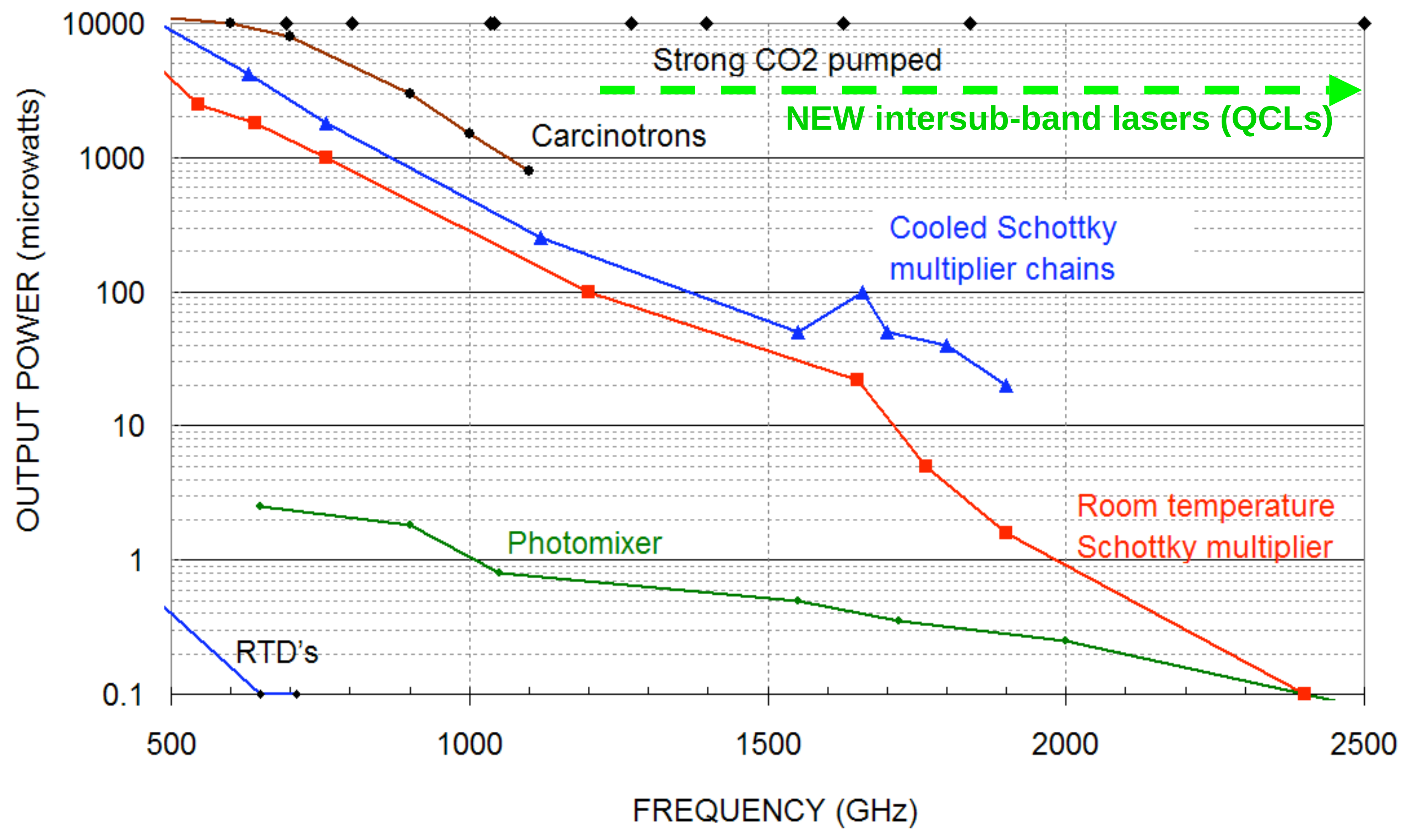
- LO for space-borne and ground-based heterodyne receivers:
  - electronically tune-able sub-millimeter and THz sources
  - Reliability / size / power consumption / temperature

Solid-State THz Sources (CW)
State-Of-The-Art



From T. Crowe et al. “Opening the THz window with integrated diode circuits”, IEEE Journal of Solid-State Circuits, Vol. 40, n°10, Oct. 2005

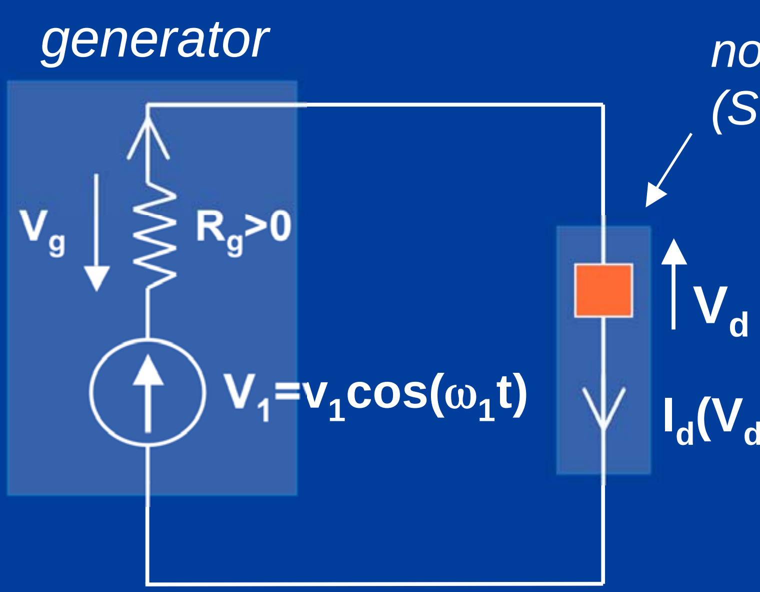
Solid-State THz Sources (CW) below 2.5 THz



Compiled by Peter Siegel, 2003, updated by Alain Maestrini, 2005

How does a frequency multiplier work ?

Non linear-device pumped with a sinusoidal signal :



non-linear device
(Schottky diode for example)

non-linear term

$I_d(V_d)=a_0+a_1V_d+a_2V_d^2$ *(for example)*

$$\begin{cases} I_d(V) = a_0 + a_1 V_d + a_2 {V_d}^2 \\ V_g = R_g \cdot I_d \\ V_d = V_1 - V_g = v_1 \cos(\omega_1 t) - R_g (a_0 + a_1 V_d + a_2 {V_d}^2) \end{cases}$$

These equations are true ∀t. When the permanent regime is reached :

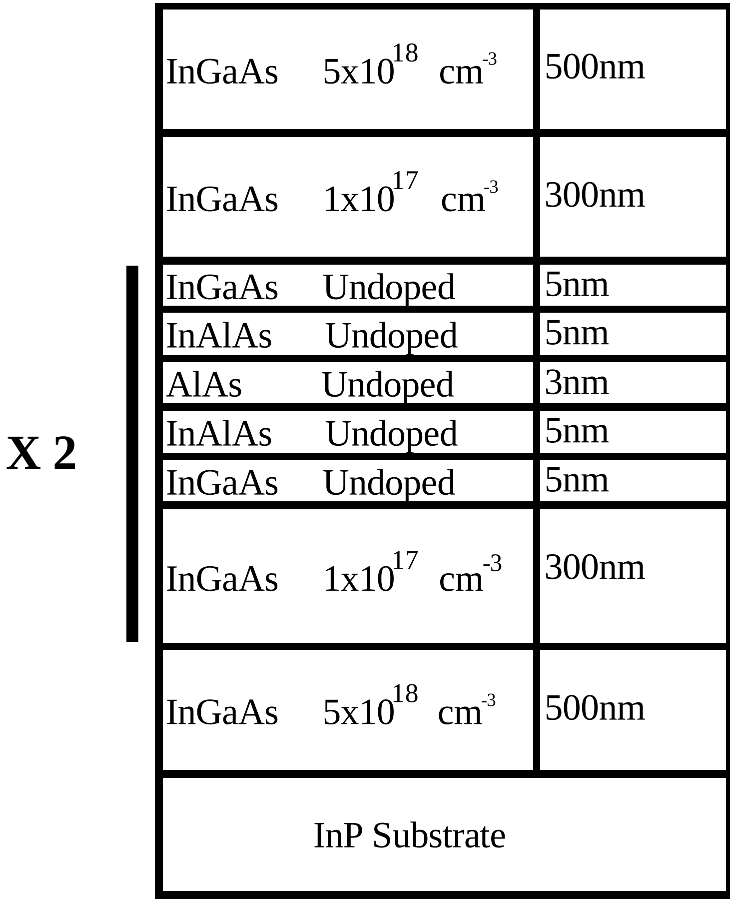
$$V_d(t) = \sum_{n\in\mathbb{N}} V_n \cos(n\cdot\omega_1\cdot t + \varphi_n)$$

Devices for
THz Frequency Multipliers

There are mainly two device technologies in competition for THz frequency multipliers :

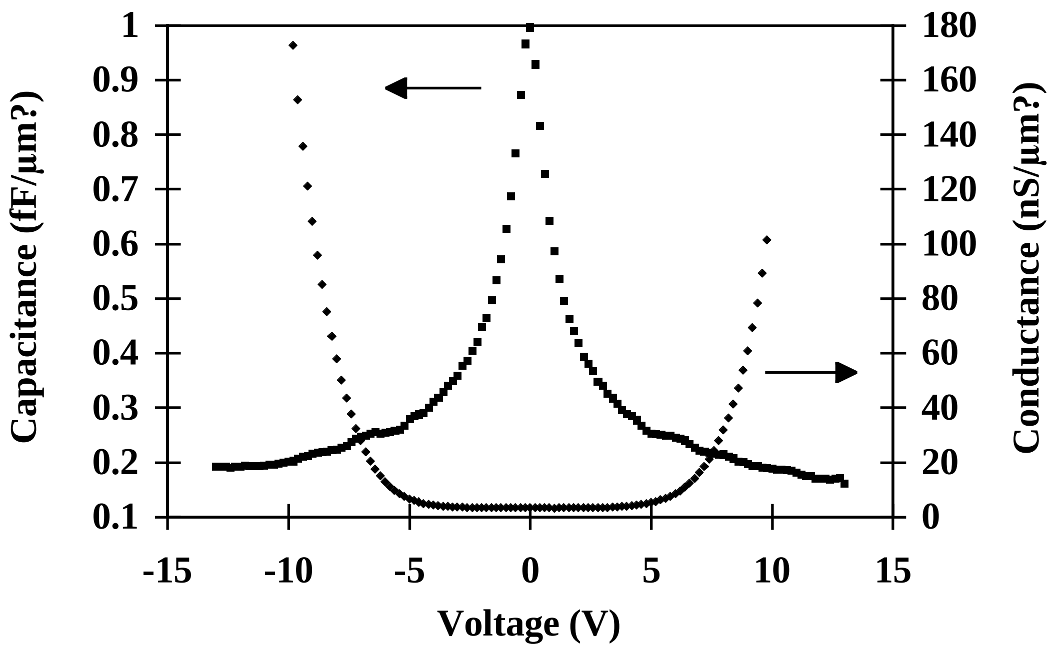
➢ Heterostructure Barier Varactor are suited for the generation of odd harmonics due to their internal symmetry:

Epitaxial layer of IEMN HBVs



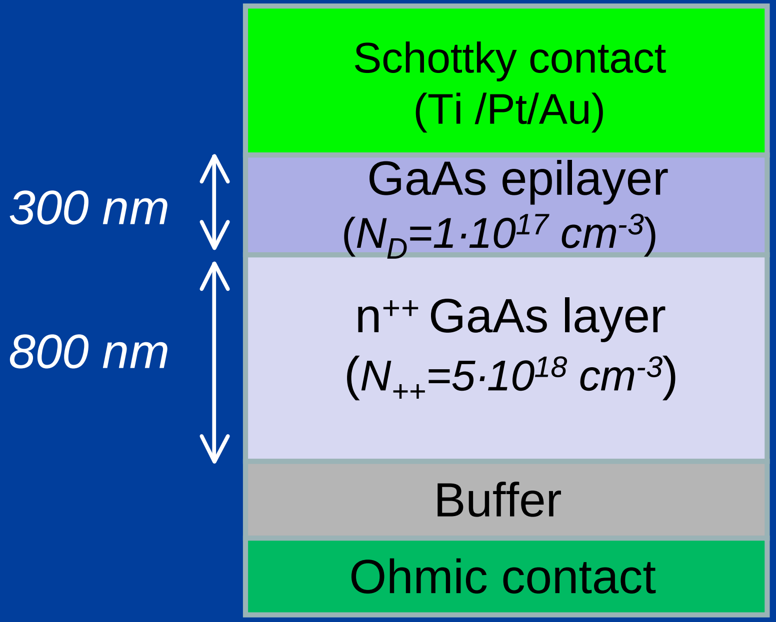
	InGaAs 5x10^{18} cm^{-3}	500nm
	InGaAs 1x10^{17} cm^{-3}	300nm
X 2	InGaAs Undoped	5nm
	InAlAs Undoped	5nm
	AlAs Undoped	3nm
	InAlAs Undoped	5nm
	InGaAs Undoped	5nm
	InGaAs 1x10^{17} cm^{-3}	300nm
	InGaAs 5x10^{18} cm^{-3}	500nm
	InP Substrate	

C(V) and I(V) curves of IEMN HBVs



Devices for THz Frequency Multipliers

- Schottky diodes are the simplest possible devices: a metal deposited on a doped semiconductor.



Schottky contact (Ti /Pt/Au)

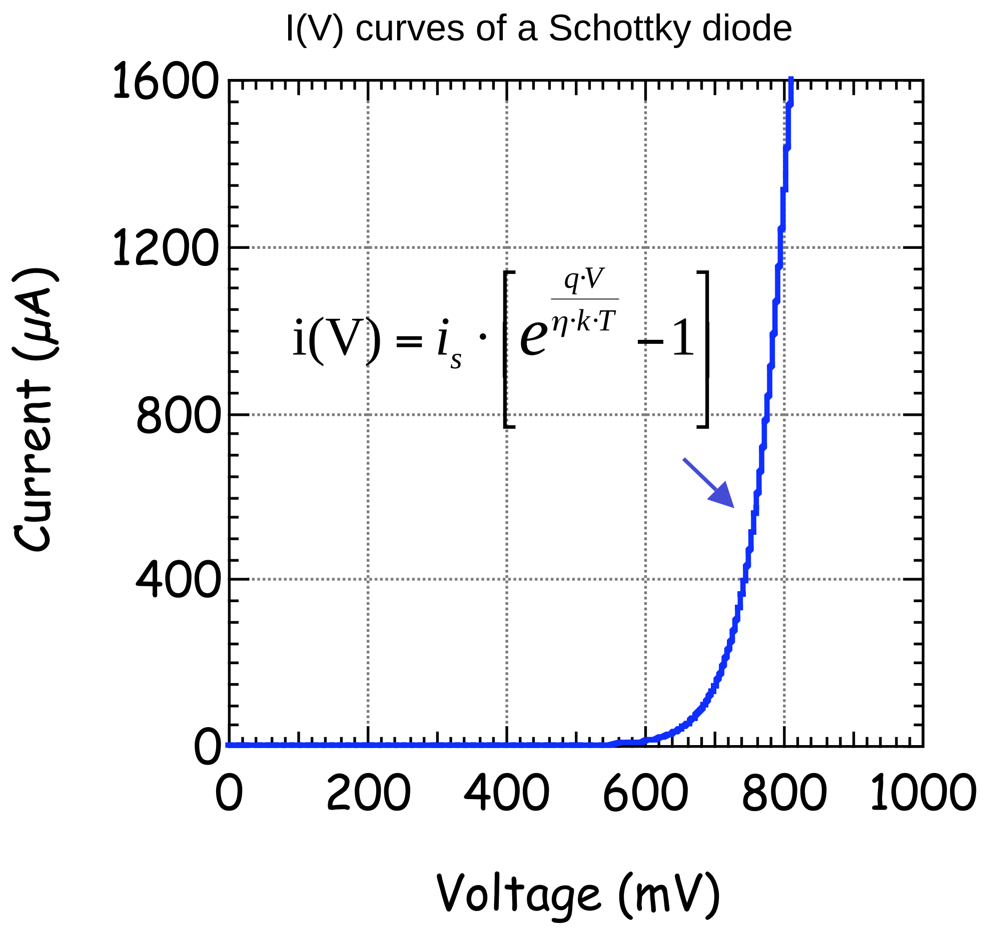
GaAs epilayer (N_D=$1 \cdot 10^{17}$ cm^{-3})

n^{++} GaAs layer (N_{++}=$5 \cdot 10^{18}$ cm^{-3})

Buffer

Ohmic contact

Epitaxial layer of a Schottky diode



I(V) curves of a Schottky diode

$$i(V) = i_s \cdot \left[e^{\frac{q \cdot V}{\eta \cdot k \cdot T}} - 1 \right]$$

Devices for THz Frequency Multipliers

- Schottky diodes are very fast devices and are (still !) the best devices for high efficiency THz frequency multipliers.

$$C_j(V) = C_j(0) \cdot \frac{1}{\sqrt{1 - V/V_b}} \quad \text{for } V < V_b$$

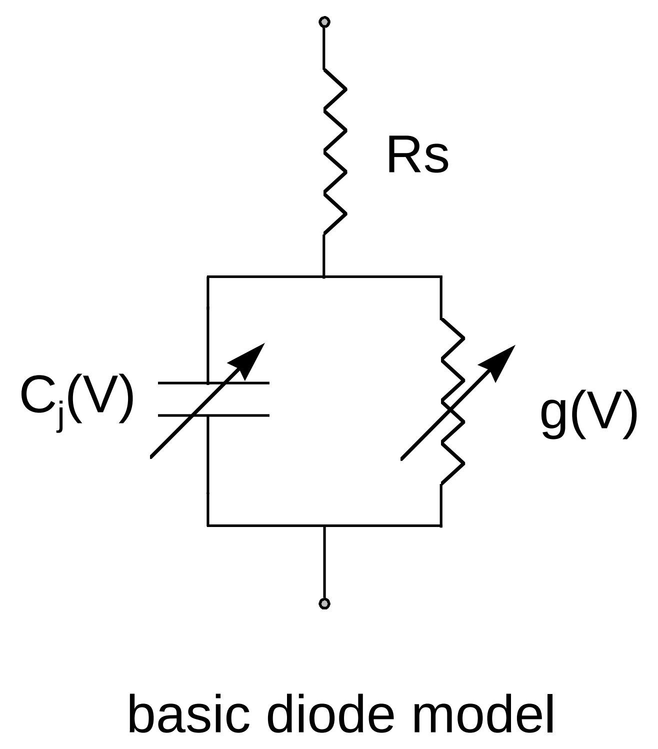
V_b is the built-in voltage.

Usualy Vb $\simeq$ 0.8V to 0.9V for GaAs diodes.

$C_j(0)$ is proportional to the anode area

(if edge effects are non-significant)

and depends on the doping.



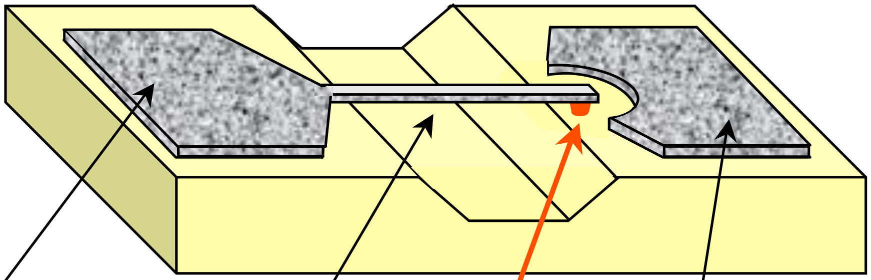
basic diode model

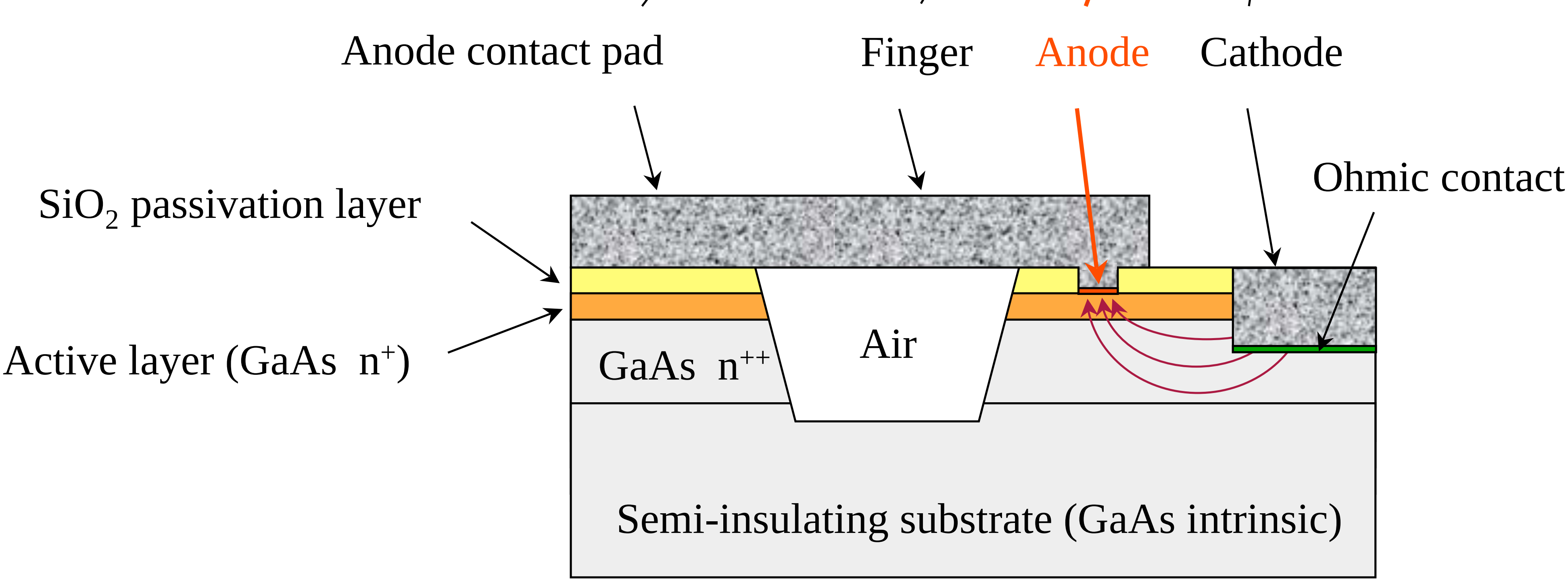
Planar Schottky diodes

Surface channel discrete planar diode (Univ. Bath then UVa - late 80’s)

Advantages

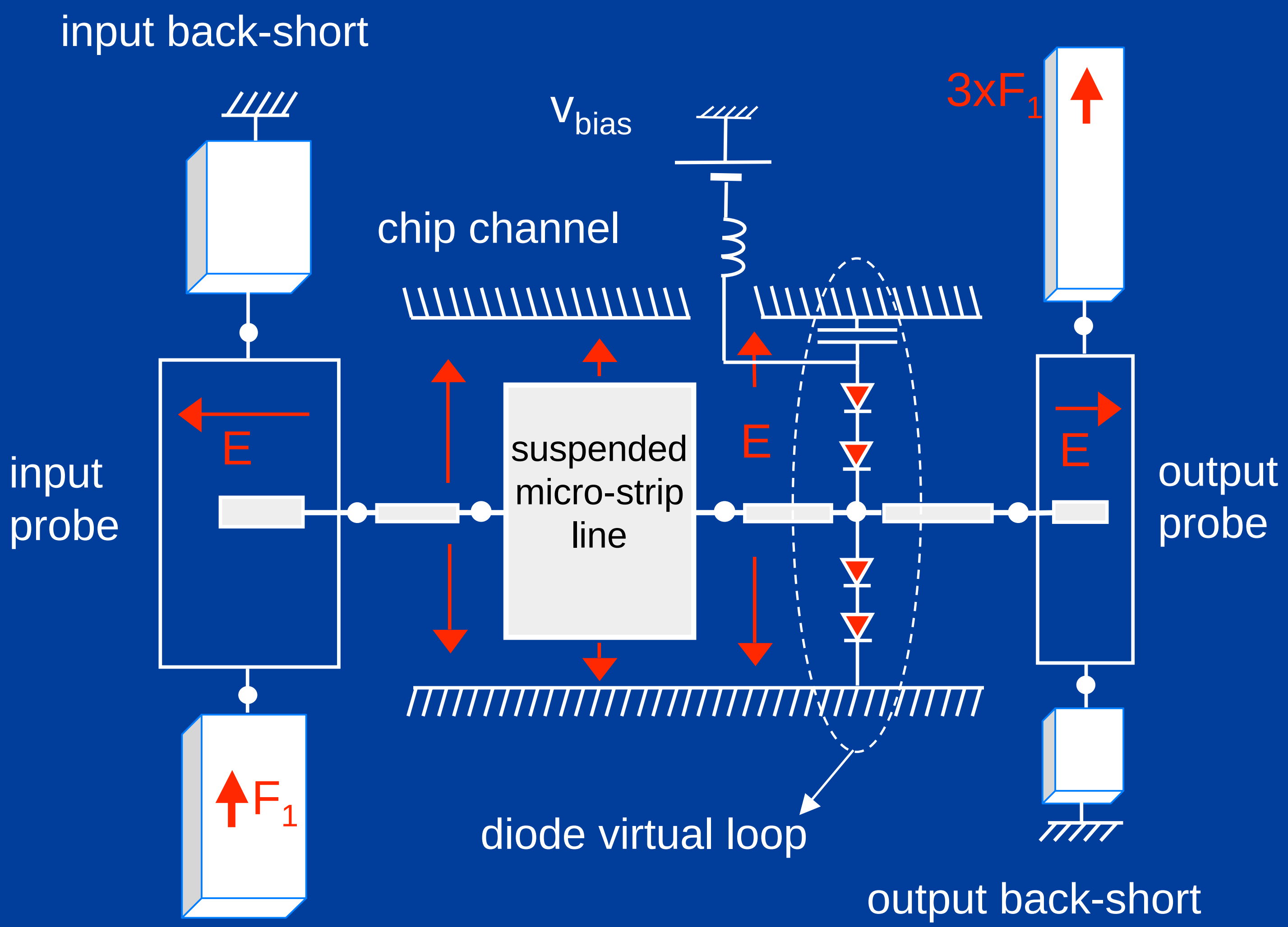
- reliability (space application)
- integration (balanced designs)
- Reproducibility (wide band designs)





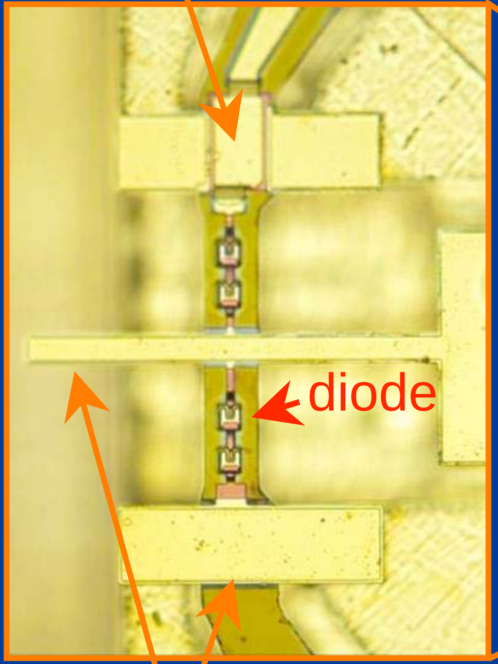
Example 1 :
540-640 GHz balanced Tripler

- Topology : balanced design, idler tuned in a virtual loop

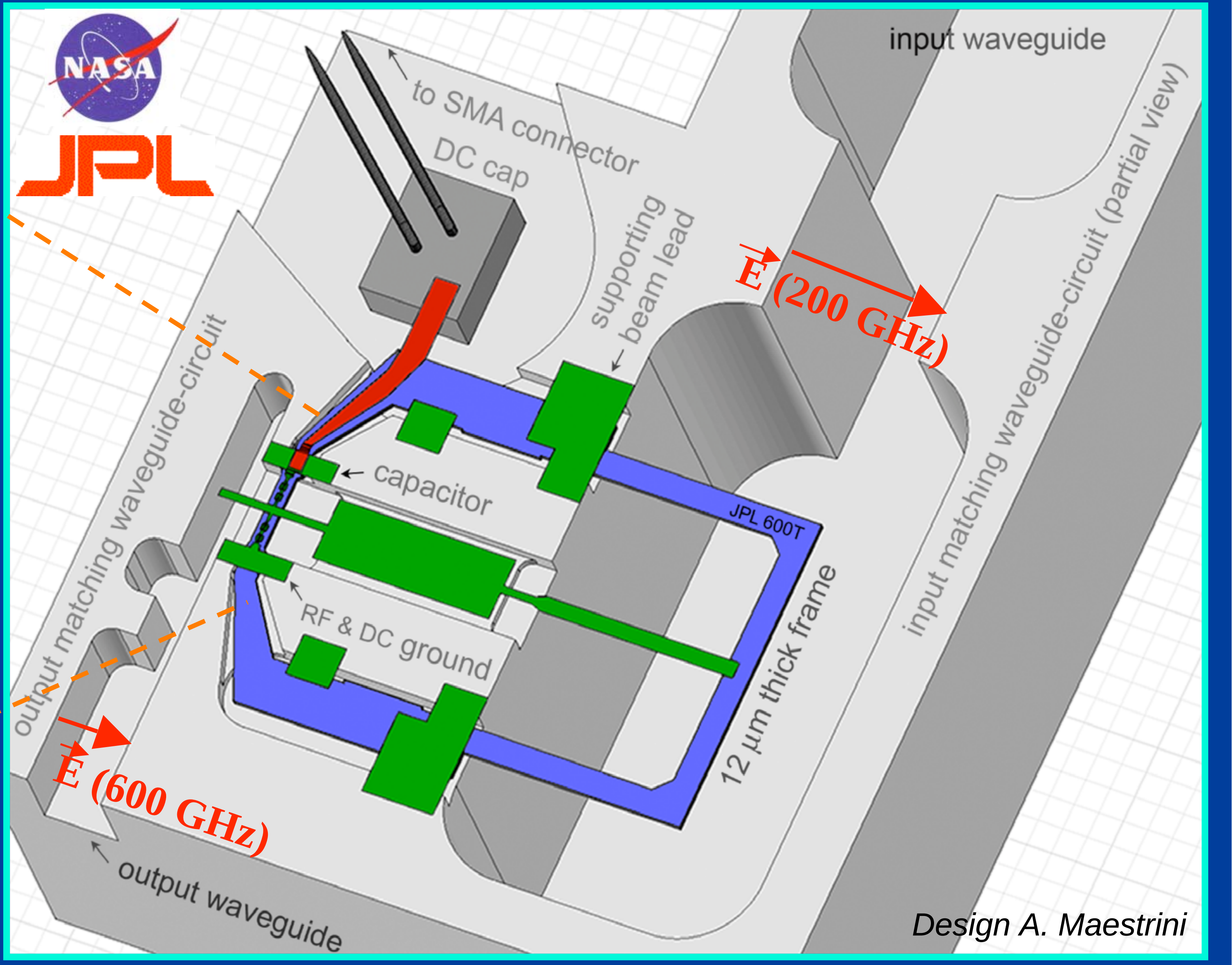


JPL 4-anode 540-640 GHz Balanced Tripler (0.8-2mW @ 300K - fully solid state - tunerless)

On-chip capacitor



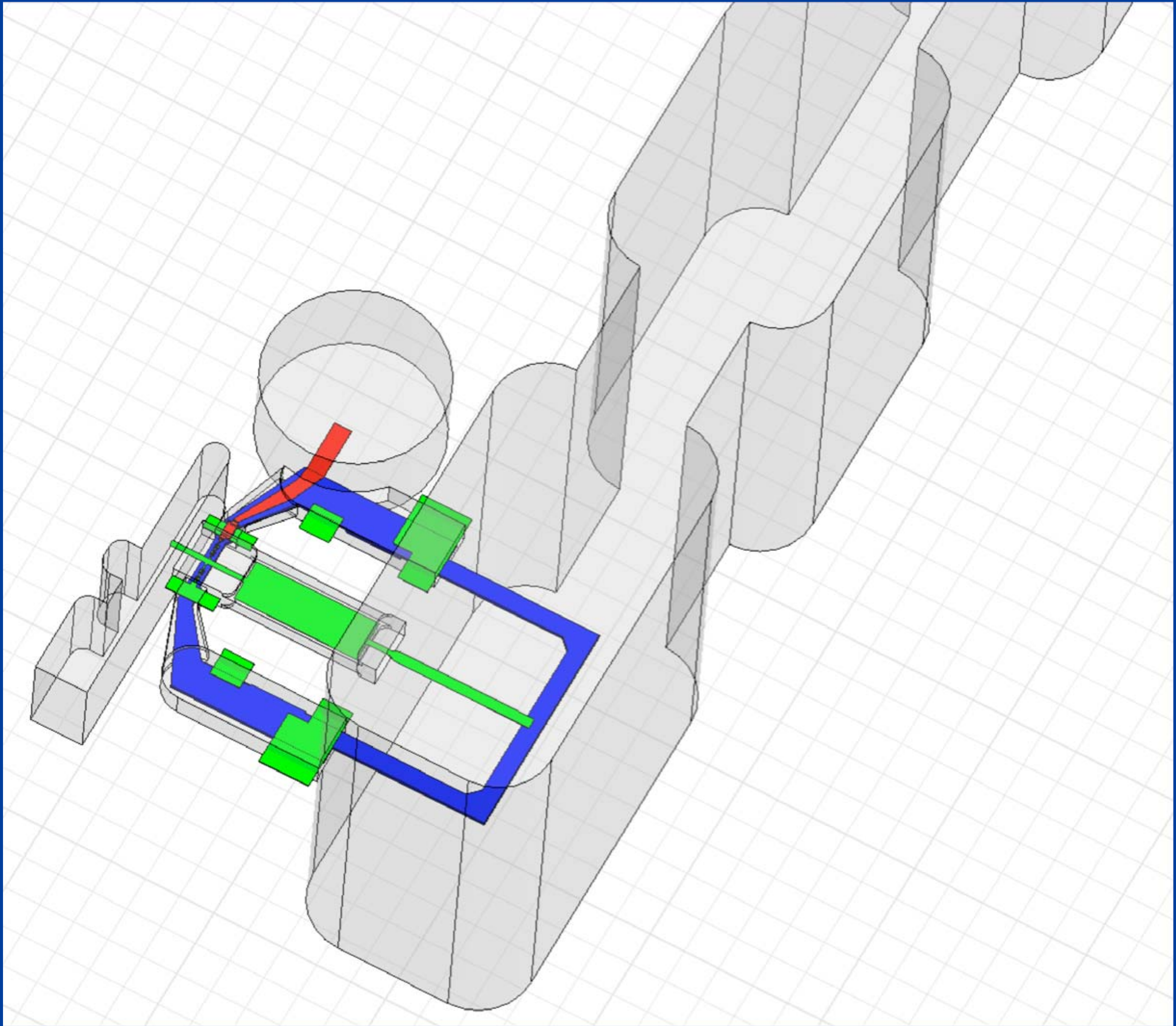
beam leads



Design A. Maestrini

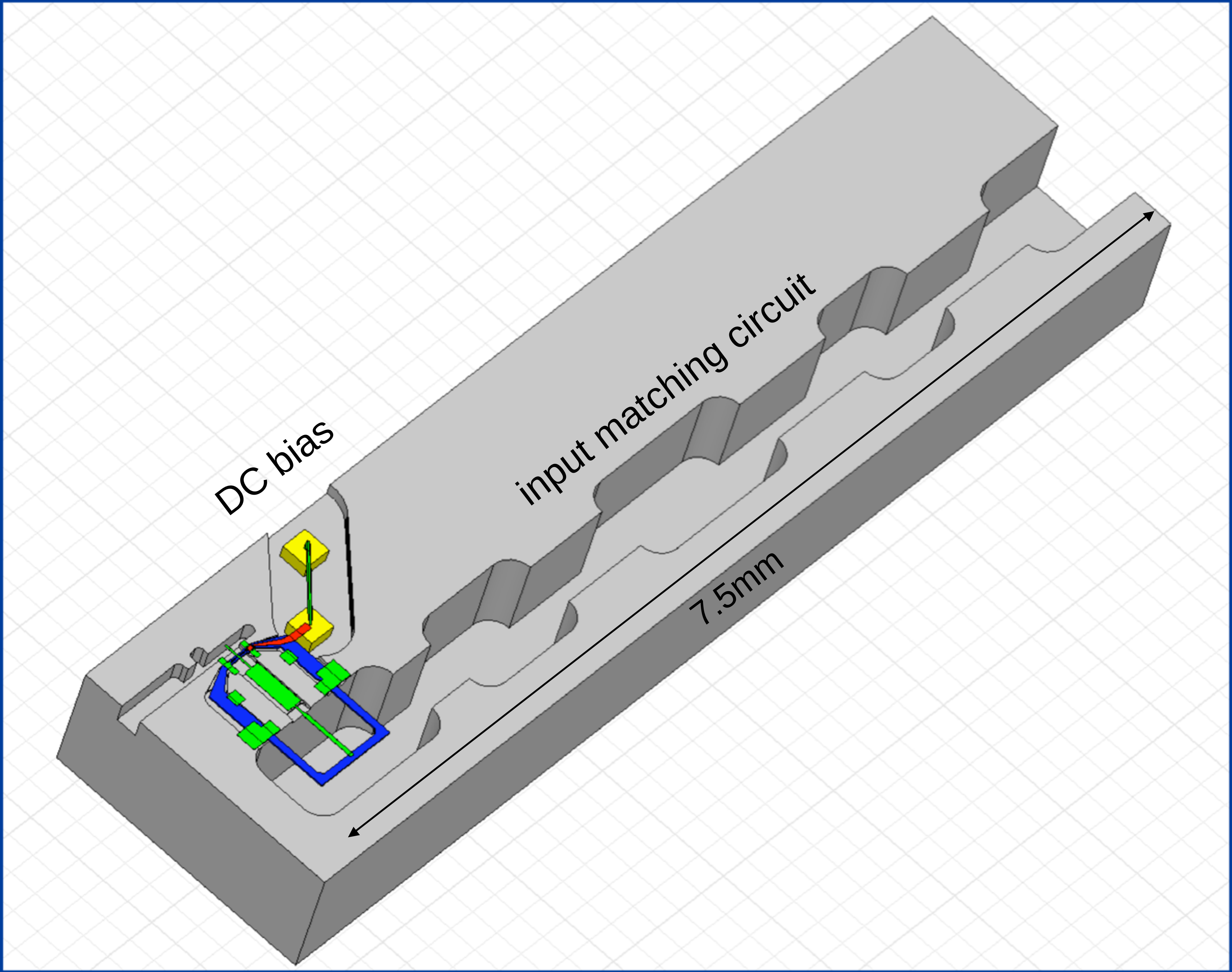
JPL 4-anode 540-640 GHz Balanced Tripler

(partial 3D view)



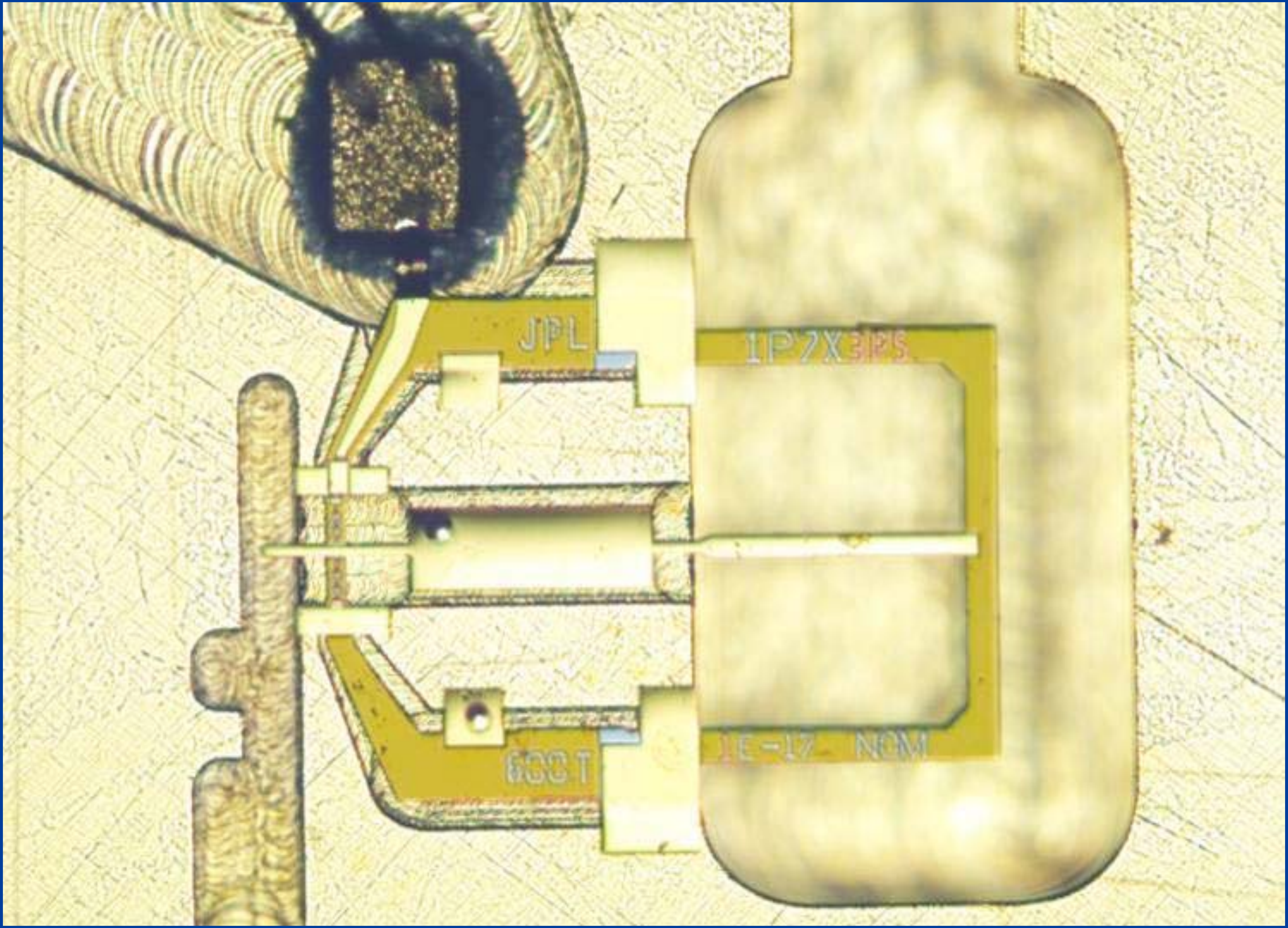
JPL 4-anode 540-640 GHz Balanced Tripler

(3D view of bottom block)

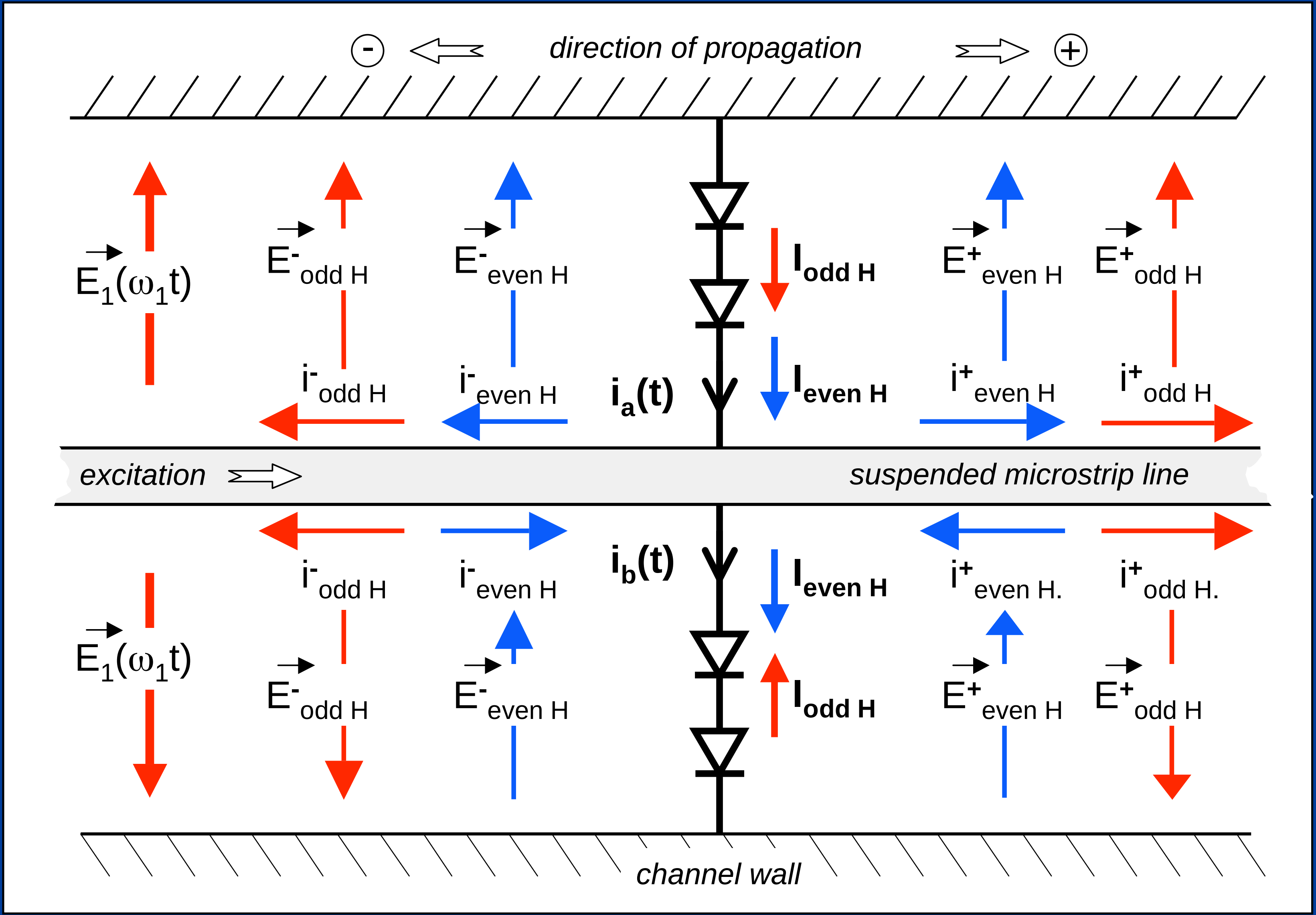


JPL 4-anode 540-640 GHz Balanced Tripler

(picture of the chip with bias circuit)



Why is the circuit balanced ?



Why is the circuit balanced ?

Due to the symmetry of the circuit and the symmetry of the excitation (input signal) :

$$i_b(t) = i_a(t + T_1 / 2) \qquad (1)$$

where T_1 is the period of the input signal

$$i_a(t) = \sum_{n=-\infty}^{+\infty} a_n e^{jn\omega_1 t} \qquad (2)$$

$$i_b(t) = \sum_{n=-\infty}^{+\infty} a_n e^{jn\omega_1 \cdot (t+T_1/2)} \qquad (3)$$

where $(a_n)_{n\in\mathbb{Z}}$, are complex coefficients that depend on the circuit and the strength of the fundamental signal. With the following notations:

$$I_{even\ \mathrm{H}} = \sum_{n=-\infty}^{+\infty} a_{2n} e^{j2n\omega_1 t} \qquad (4)$$

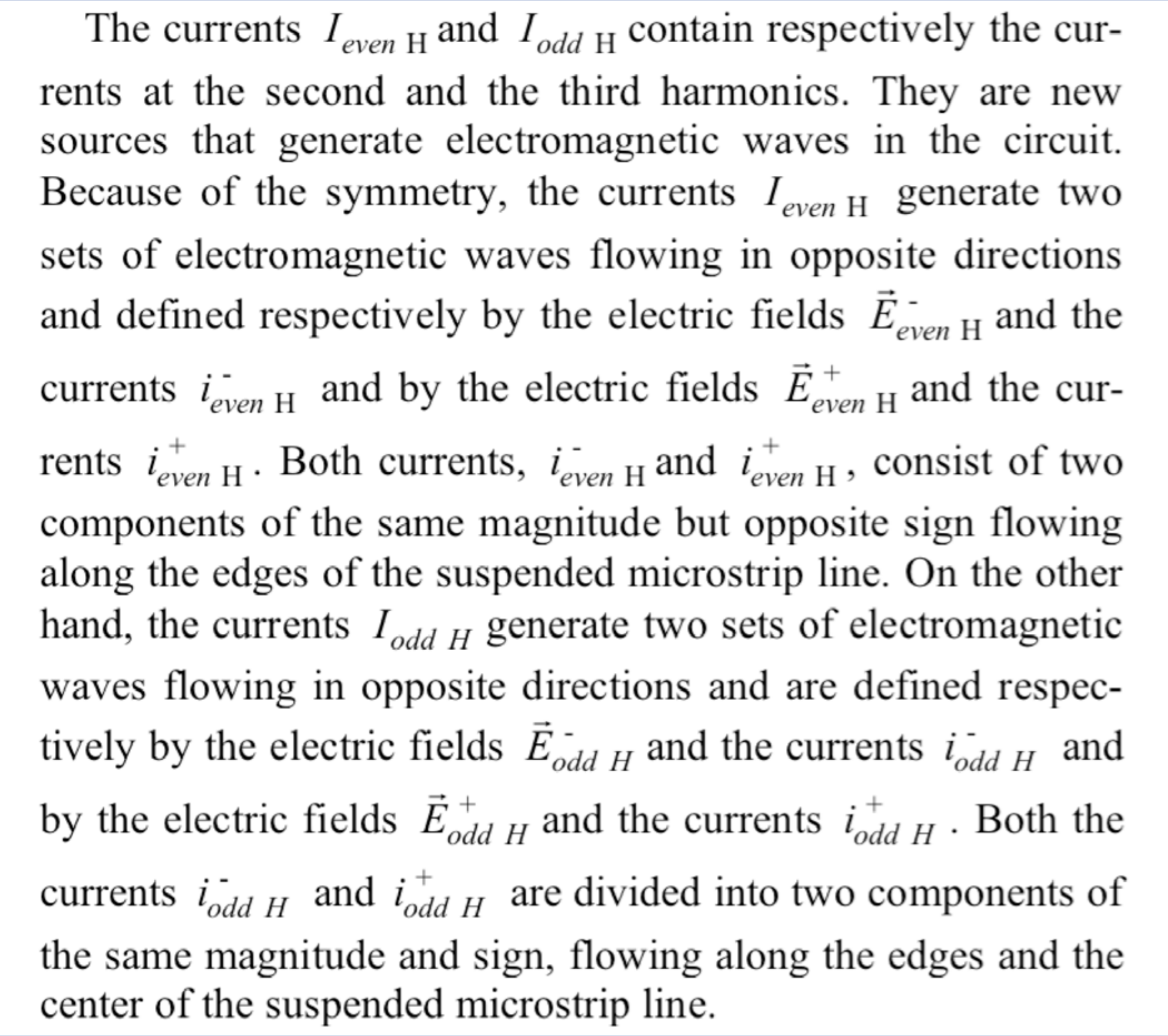
$$I_{odd\ \mathrm{H}} = \sum_{n=-\infty}^{+\infty} a_{2n+1} e^{j(2n+1)\omega_1 t} \qquad (5)$$

equations (2) and (3) bocome :

$$i_a(t) = I_{even\ \mathrm{H}} + I_{odd\ \mathrm{H}} \qquad (6)$$

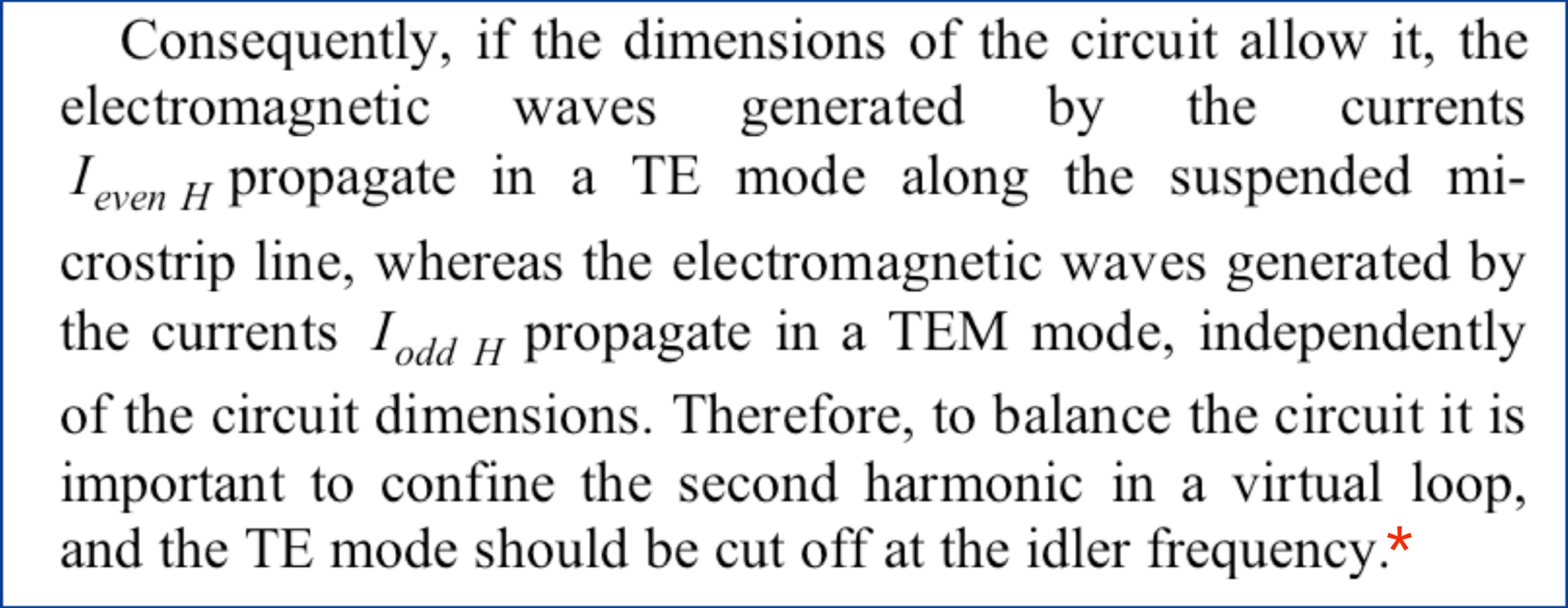
$$i_b(t) = I_{even\ \mathrm{H}} - I_{odd\ \mathrm{H}} \qquad (7)$$

Why is the circuit balanced ?



The currents $I_{even\ \mathrm{H}}$ and $I_{odd\ \mathrm{H}}$ contain respectively the currents at the second and the third harmonics. They are new sources that generate electromagnetic waves in the circuit. Because of the symmetry, the currents $I_{even\ \mathrm{H}}$ generate two sets of electromagnetic waves flowing in opposite directions and defined respectively by the electric fields $\vec{E}^{\,-}_{even\ \mathrm{H}}$ and the currents $i^{-}_{even\ \mathrm{H}}$ and by the electric fields $\vec{E}^{\,+}_{even\ \mathrm{H}}$ and the currents $i^{+}_{even\ \mathrm{H}}$. Both currents, $i^{-}_{even\ \mathrm{H}}$ and $i^{+}_{even\ \mathrm{H}}$, consist of two components of the same magnitude but opposite sign flowing along the edges of the suspended microstrip line. On the other hand, the currents $I_{odd\ H}$ generate two sets of electromagnetic waves flowing in opposite directions and are defined respectively by the electric fields $\vec{E}^{\,-}_{odd\ H}$ and the currents $i^{-}_{odd\ H}$ and by the electric fields $\vec{E}^{\,+}_{odd\ H}$ and the currents $i^{+}_{odd\ H}$. Both the currents $i^{-}_{odd\ H}$ and $i^{+}_{odd\ H}$ are divided into two components of the same magnitude and sign, flowing along the edges and the center of the suspended microstrip line.

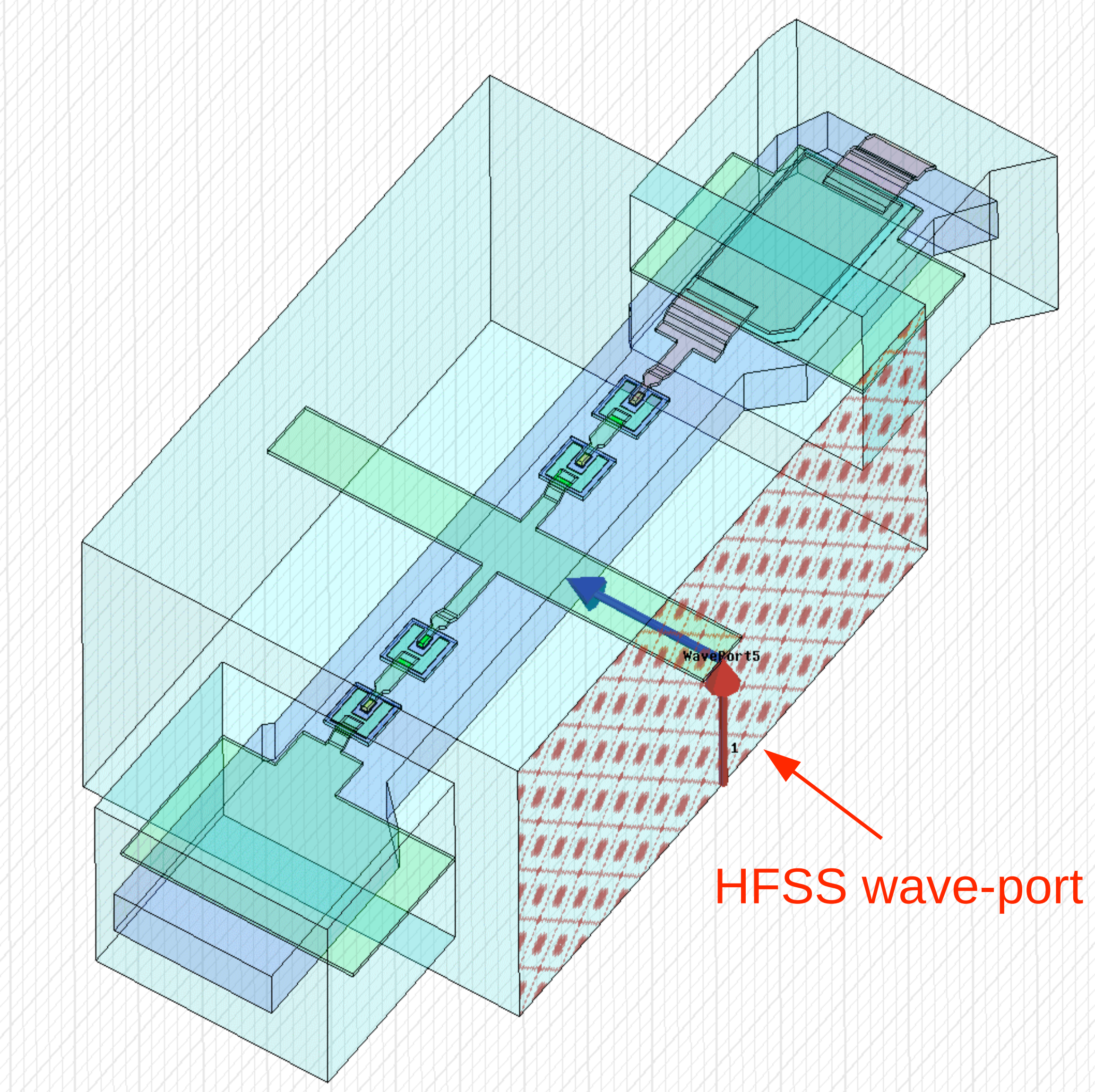
Why is the circuit balanced ?



Consequently, if the dimensions of the circuit allow it, the electromagnetic waves generated by the currents $I_{even\ H}$ propagate in a TE mode along the suspended microstrip line, whereas the electromagnetic waves generated by the currents $I_{odd\ H}$ propagate in a TEM mode, independently of the circuit dimensions. Therefore, to balance the circuit it is important to confine the second harmonic in a virtual loop, and the TE mode should be cut off at the idler frequency.*

* The idler frequency for a frequency tripler is the second harmonic of the input signal

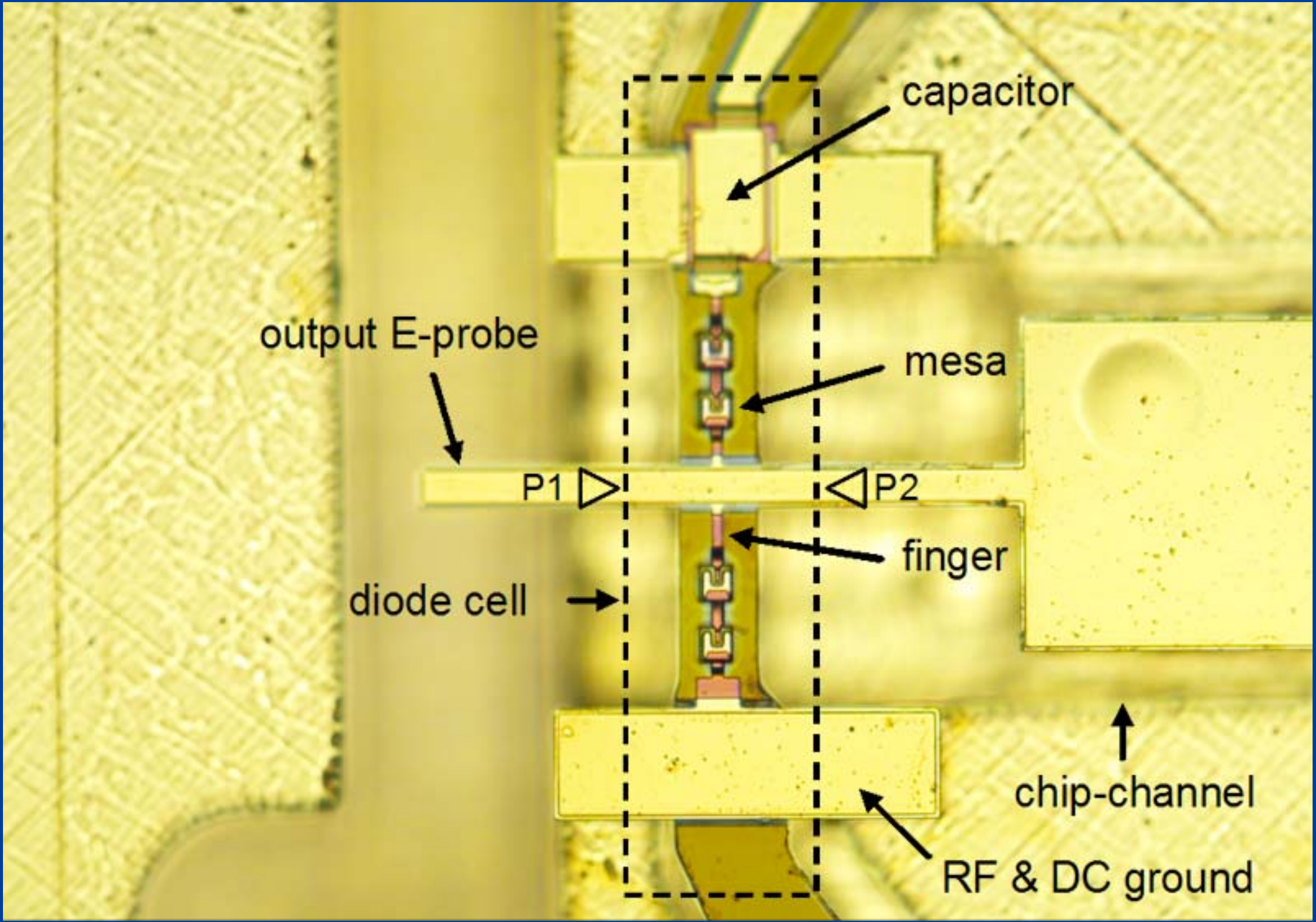
Design Method : optimizing the diode cell



Optimizing the diode cell and anode area of the 540-640GHz tripler (doping=1^{E}17cm^{-3}, Cj0≈5.7fF each)

Design Method : optimizing the diode cell

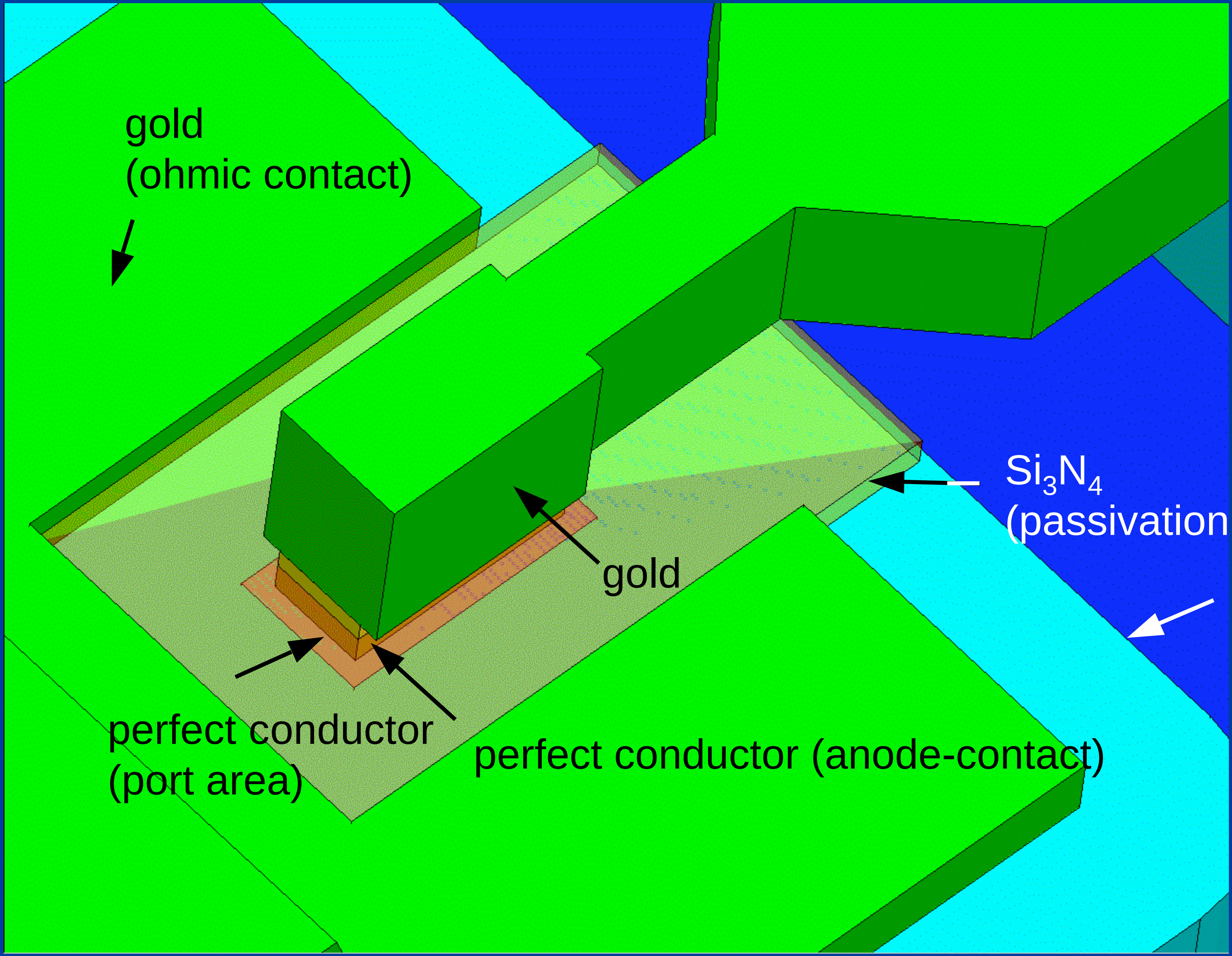
Picture of the multiplier



Optimizing the diode cell and anode area of the 540-640GHz tripler (doping=$1^{E}17cm^{-3}$, Cj0≈5.7fF each)

HFFS – Diode model

for JPL diodes



gold (ohmic contact)

Si_3N_4 (passivation layer)

gold

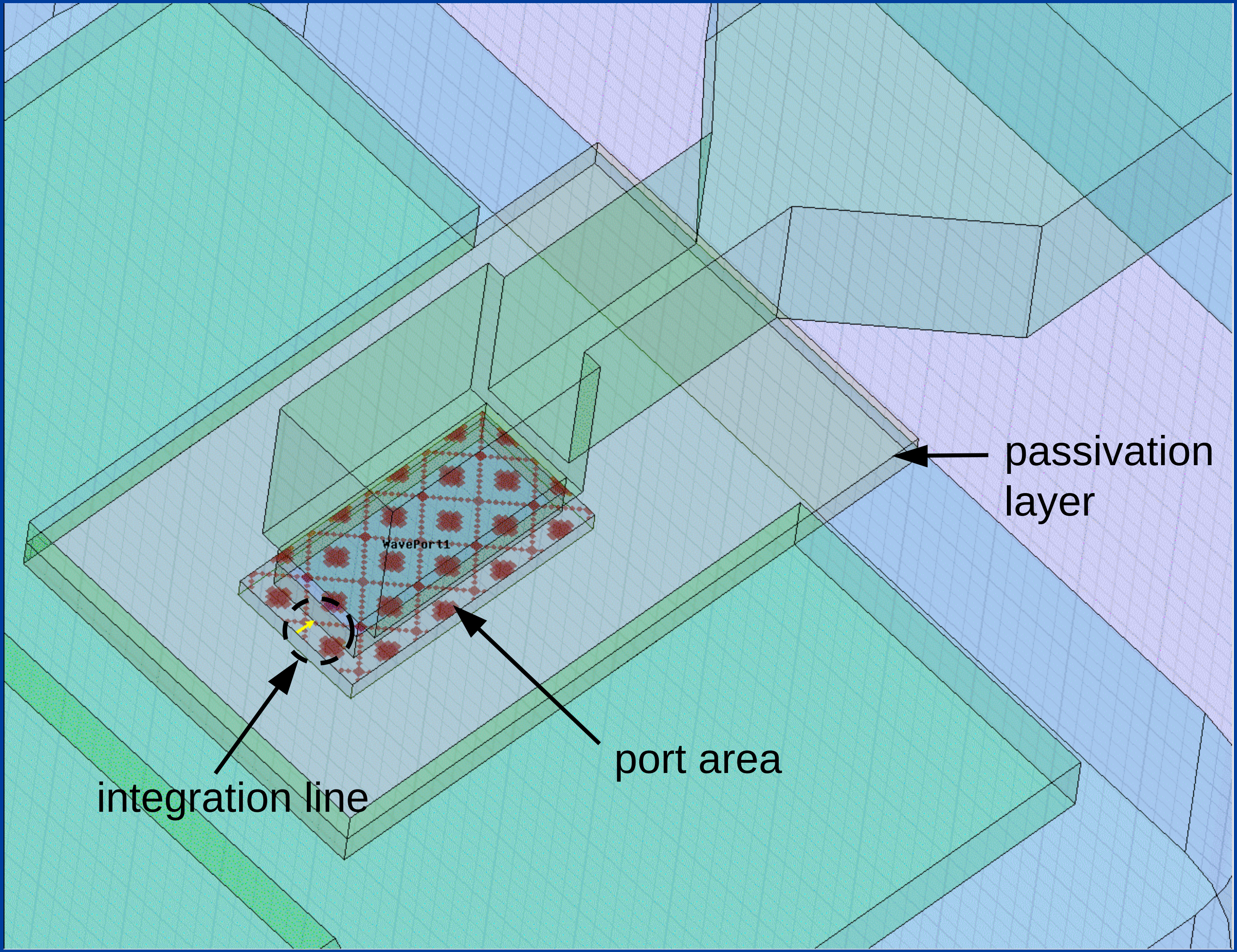
lossy metal (mesa)

perfect conductor (port area)

perfect conductor (anode-contact)

HFFS – port definition

for JPL diodes

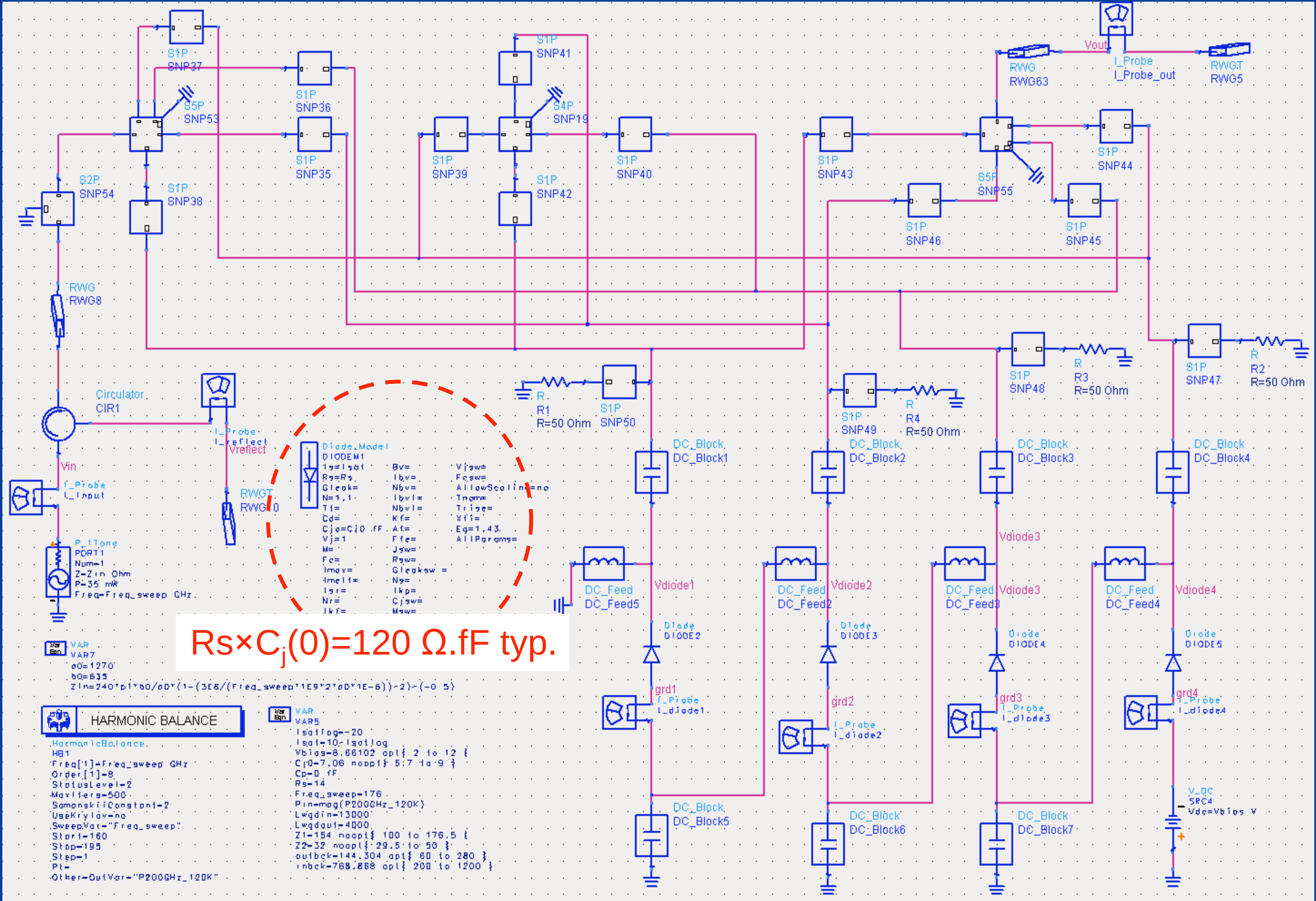


passivation layer

port area

integration line

ADS Diode Model



```
Diode_Model
DIODEM1
Is=Isat        Bv=           Vjsw=
Rs=Rs          Ibv=          Fcsw=
Gleak=         Nbv=          AllowScaling=no
N=1.1          Ibvl=         Tnom=
Tt=            Nbvl=         Trise=
Cd=            Kf=           Xti=
Cjo=Cj0 fF     Af=           Eg=1.43
Vj=1           Ffe=          AllParams=
M=             Jsw=
Fc=            Rsw=
Imax=          Gleaksw =
Imelt=         Ns=
Isr=           Ikp=
Nr=            Cjsw=
Ikf=           Msw=
```

Rs×C_j(0)=120 Ω.fF typ.

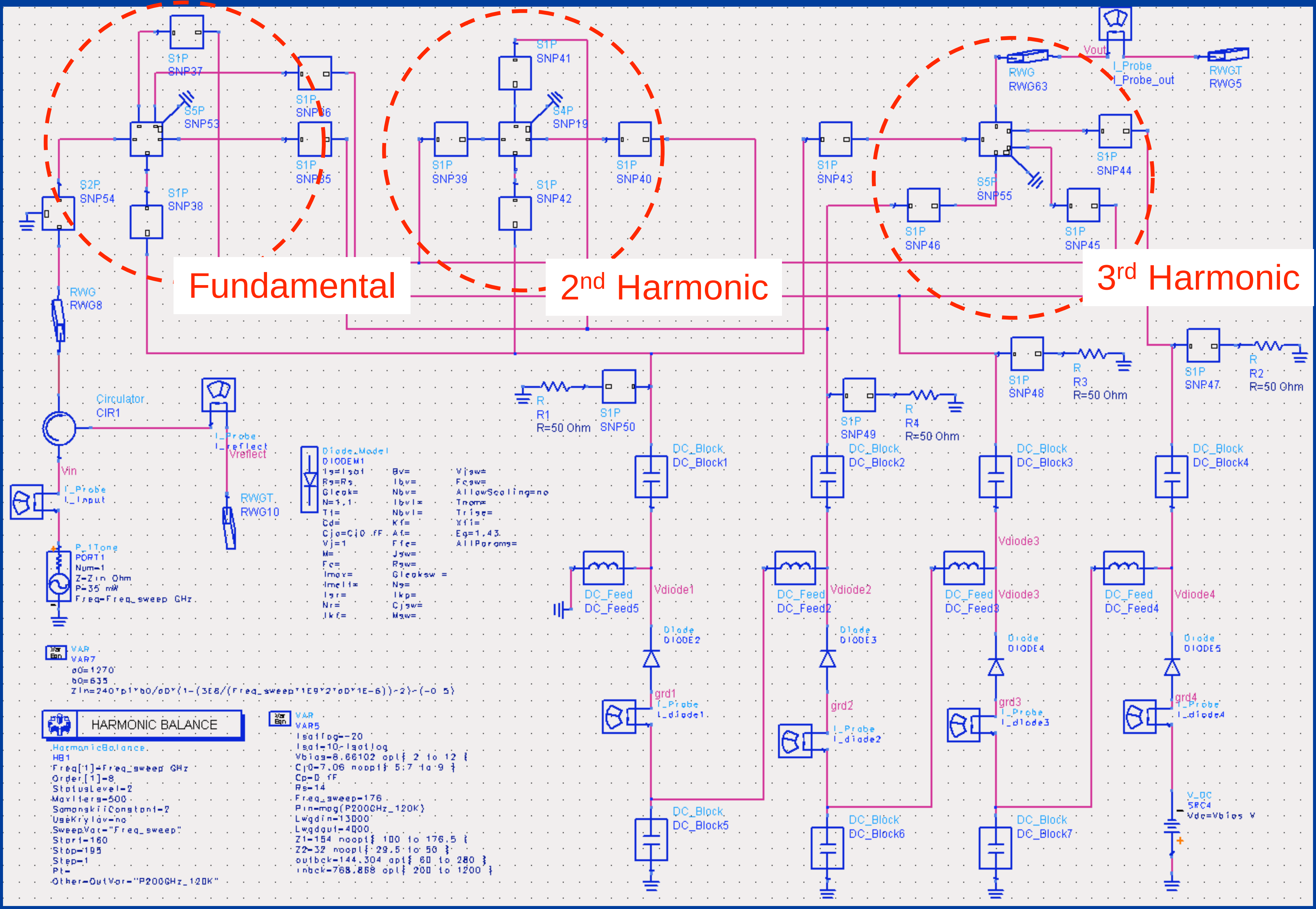
```
P_1Tone
PORT1
Num=1
Z=Zin Ohm
P=35 mW
Freq=Freq_sweep GHz
```

```
VAR
VAR7
a0=1270
b0=635
Zin=240*pi*b0/a0*(1-(3E8/(Freq_sweep*1E9*2*a0*1E-6))^2)^(-0.5)
```

```
HarmonicBalance
HB1
Freq[1]=Freq_sweep GHz
Order[1]=8
StatusLevel=2
MaxIters=500
SamanskiiConstant=2
UseKrylov=no
SweepVar="Freq_sweep"
Start=160
Stop=195
Step=1
Pt=
OtherOutVar="P200GHz_120K"
```

```
VAR
VAR5
Isatlog=-20
Isat=10^Isatlog
Vbias=8.66102 opt{ 2 to 12 }
Cj0=7.06 noopt{ 5.7 to 9 }
Cp=0 fF
Rs=14
Freq_sweep=176
Pin=mag(P200GHz_120K)
Lwgdin=13000
Lwgdout=4000
Z1=154 noopt{ 100 to 176.5 }
Z2=32 noopt{ 29.5 to 50 }
outbck=144.304 opt{ 60 to 280 }
inbck=768.868 opt{ 200 to 1200 }
```

ADS simulations with S-parameters calculated with HFSS for each harmonic



Fundamental

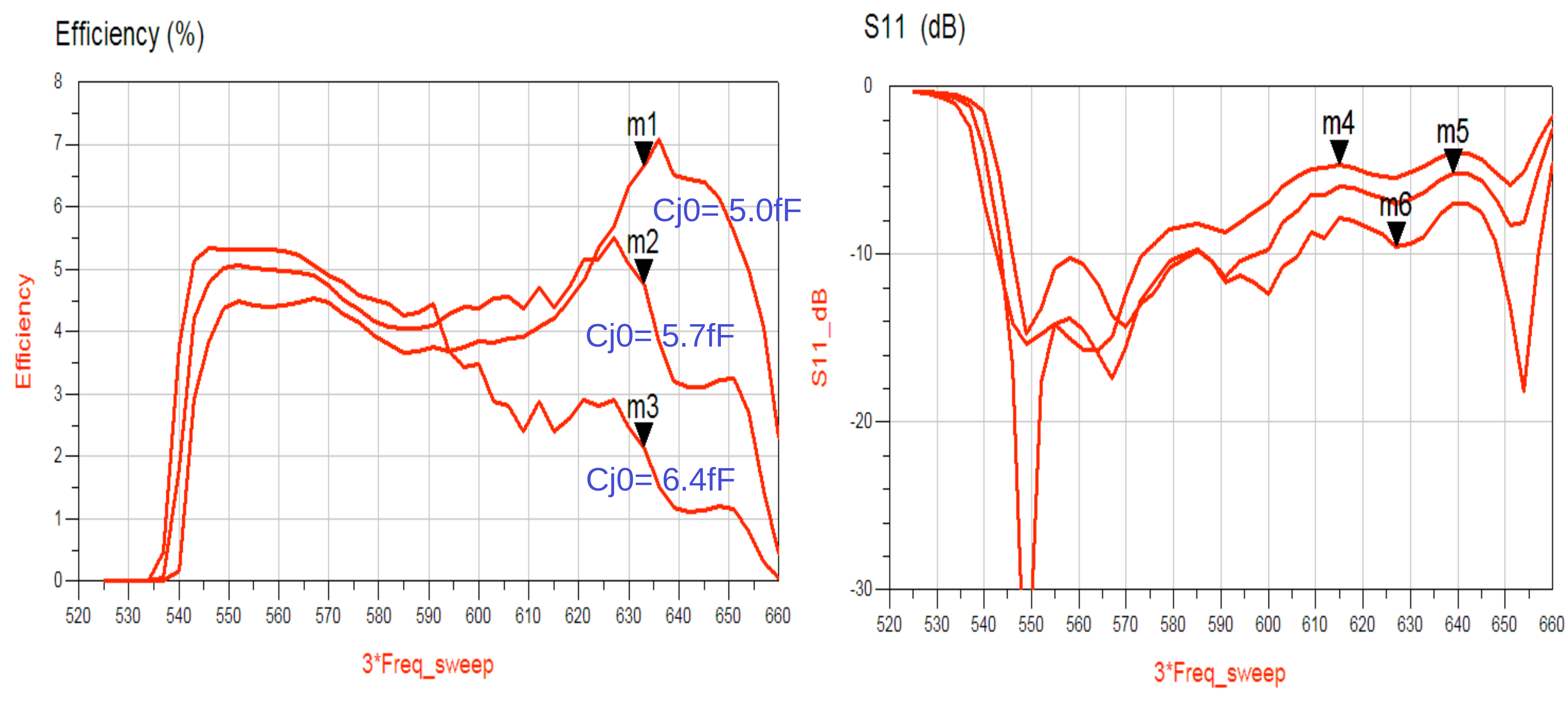
2nd Harmonic

3rd Harmonic

Impact of Cj0 on the bandwidth of the multiplier and impact on the choice of circuit variations

(JPL 600 GHz balanced Tripler)

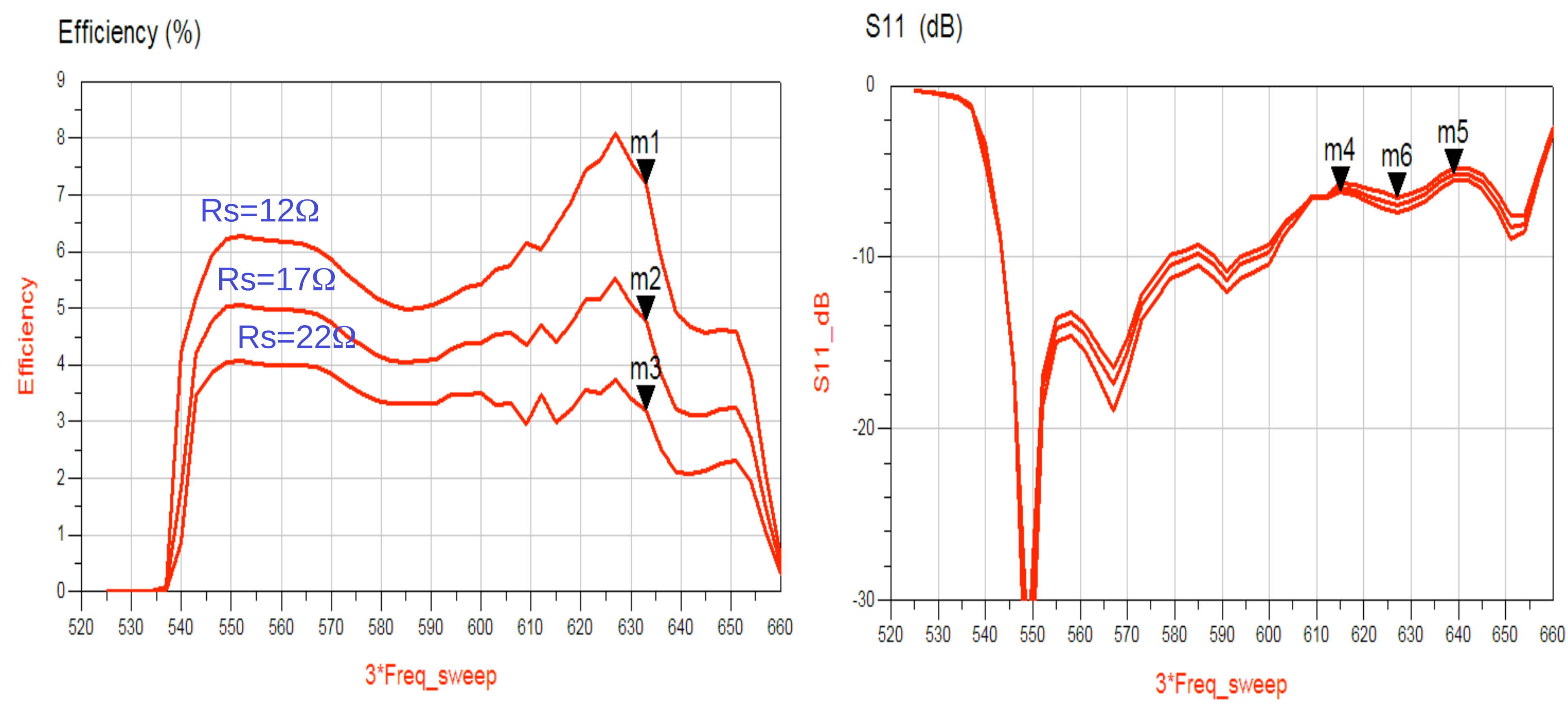
PERFORMANCE vs Cj0 :
Chips and circuits only differ by the size of the anodes



Impact of Rs on the bandwidth of the multiplier and impact on the choice of circuit variations

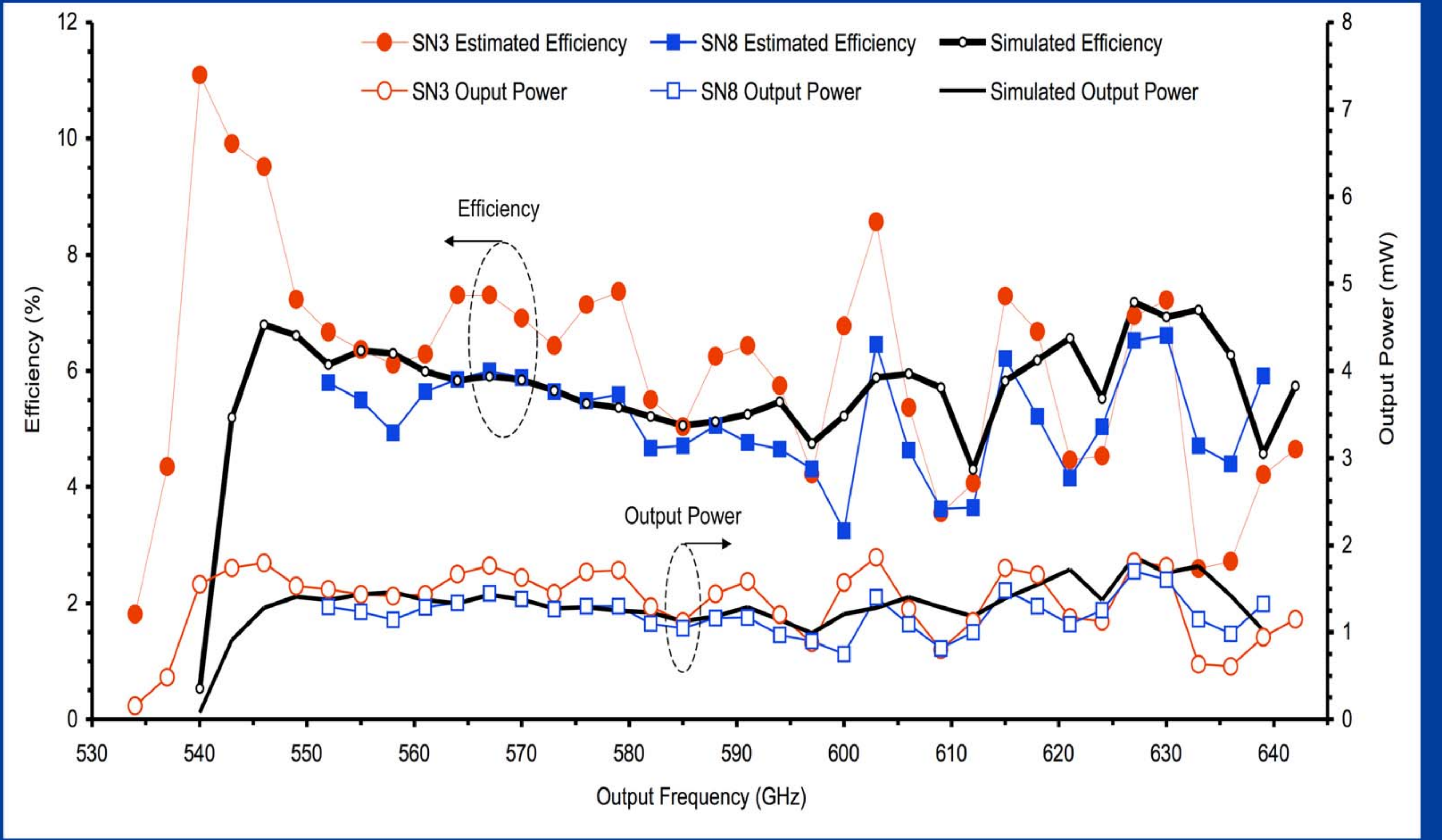
(JPL 600 GHz balanced Tripler)

PERFORMANCE vs Rs :
Chips and circuits only differ by the series resistance of the diodes



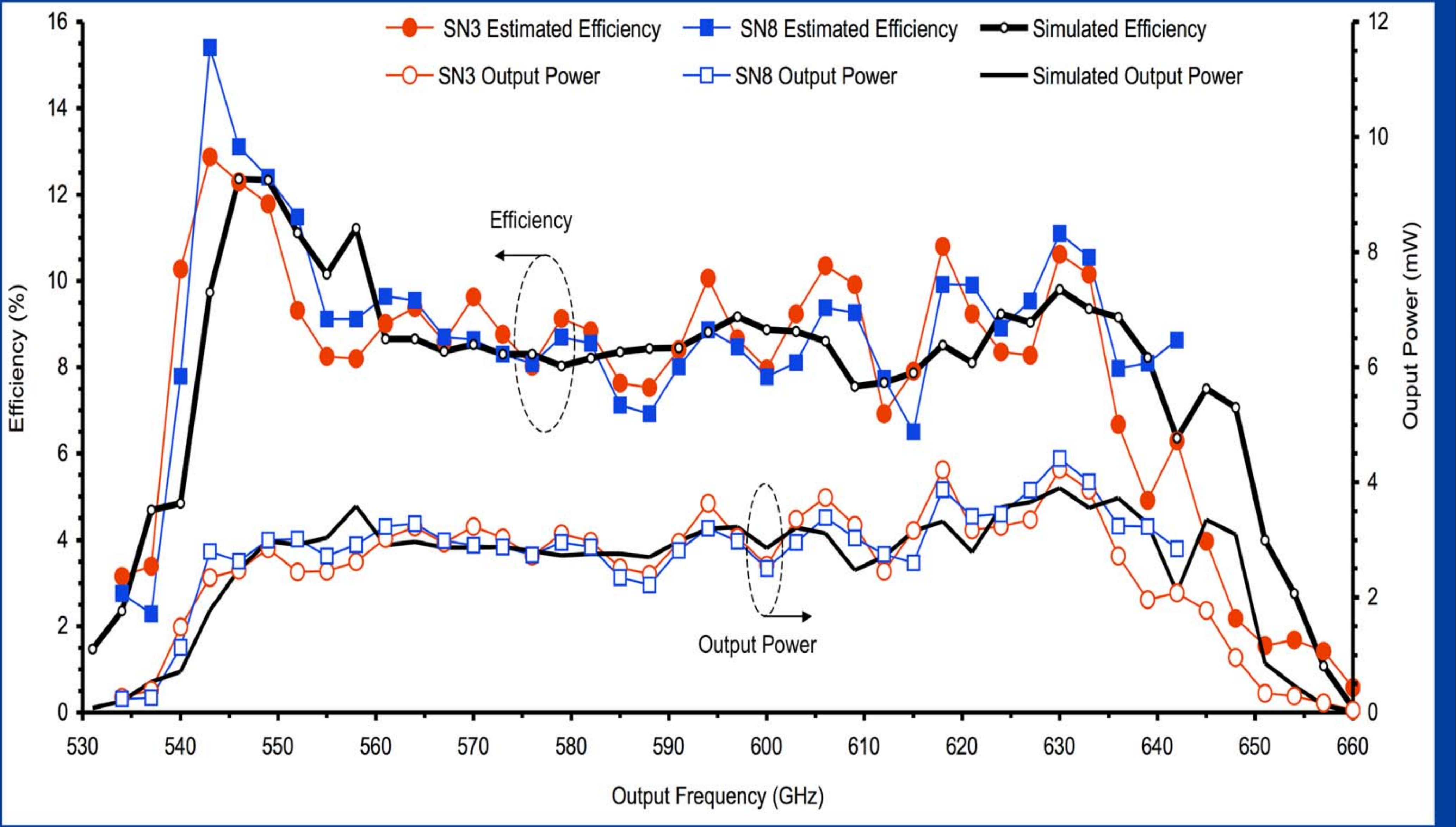
Simulations vs Measurements @T=300K

Output Power and Efficiency at 300K of two 600 GHz Balanced Triplers

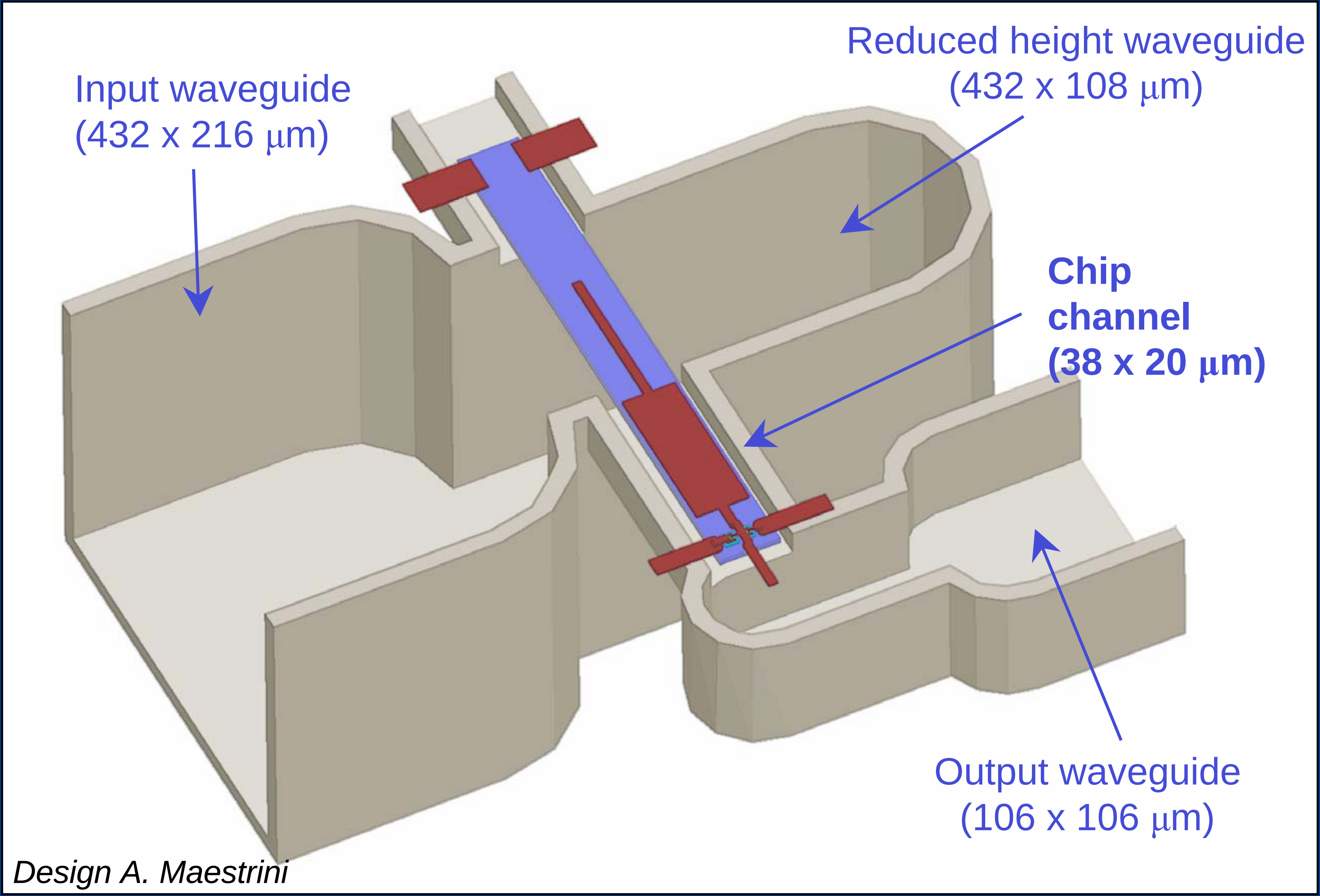


Simulations vs Measurements @T=120K

Output Power and Efficiency at 120K of two 600 GHz Balanced Triplers



Example 2 :
1.9THz balanced tripler biasless
3D view of bottom block


Input waveguide
(432 x 216 μm)

Reduced height waveguide
(432 x 108 μm)

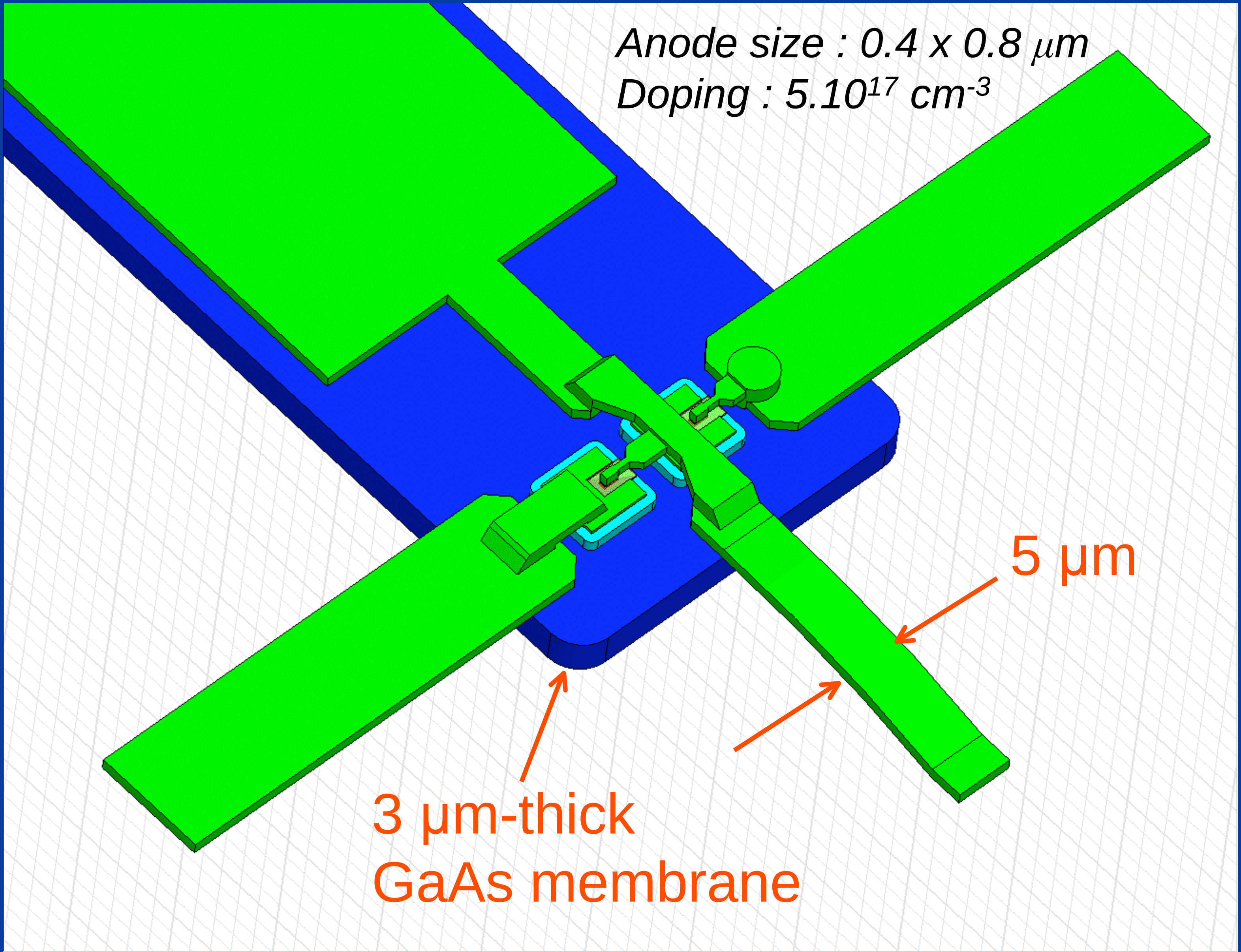
**Chip channel
(38 x 20 μm)**

Output waveguide
(106 x 106 μm)

Design A. Maestrini

1.9THz balanced tripler biasless

(detail of the chip)



Anode size : 0.4 x 0.8 μm

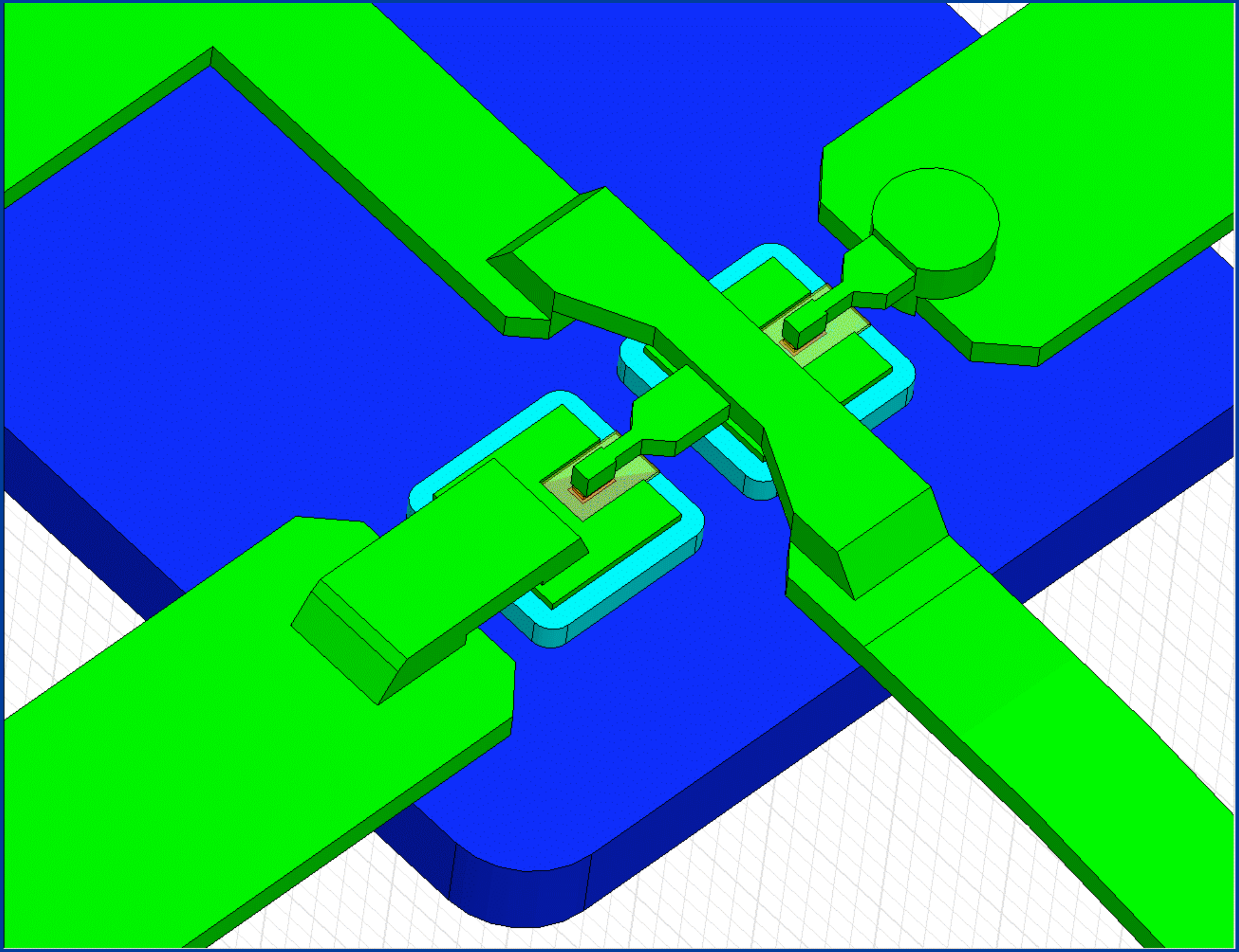
Doping : 5.10^{17} cm^{-3}

5 µm

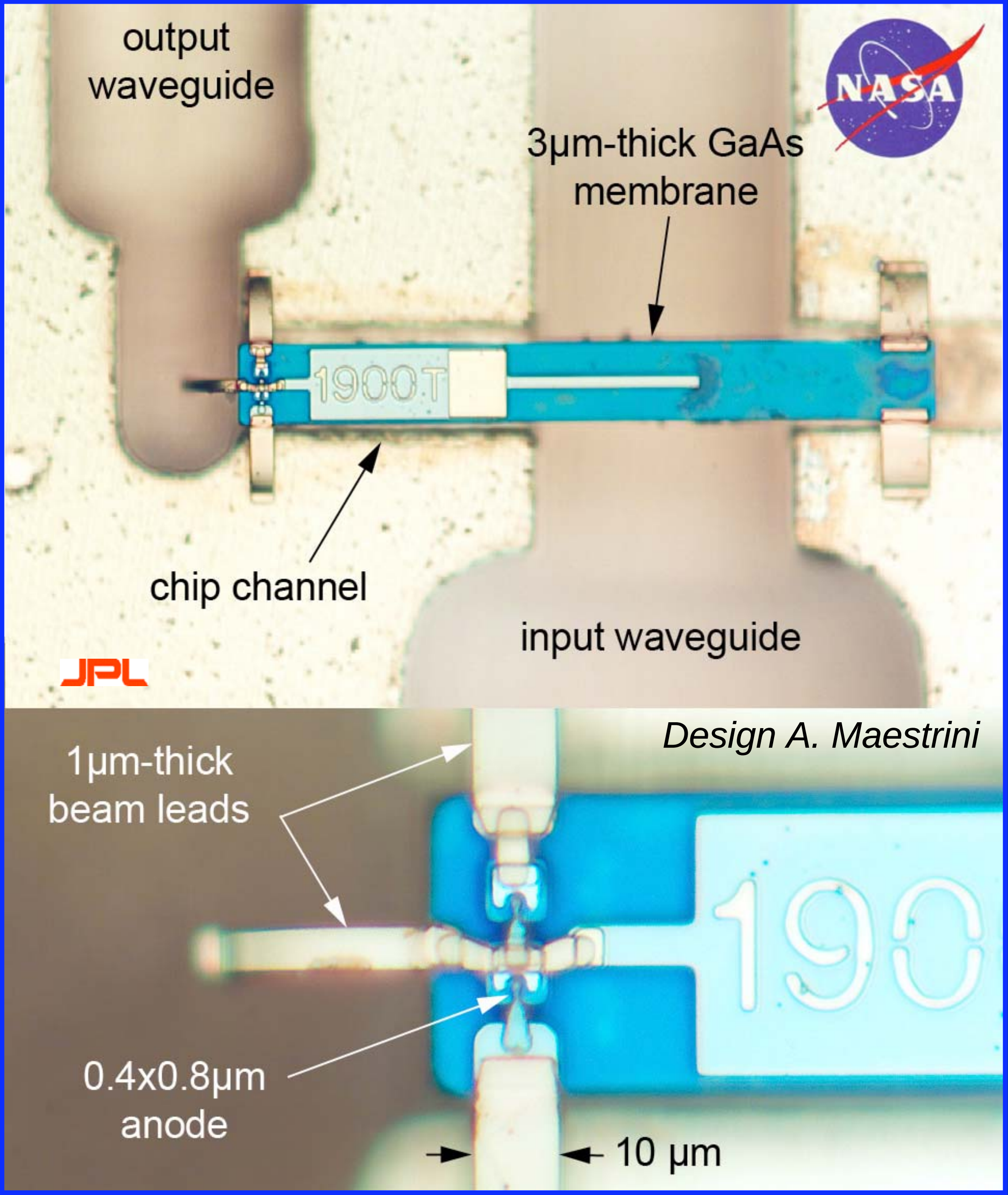
3 µm-thick
GaAs membrane

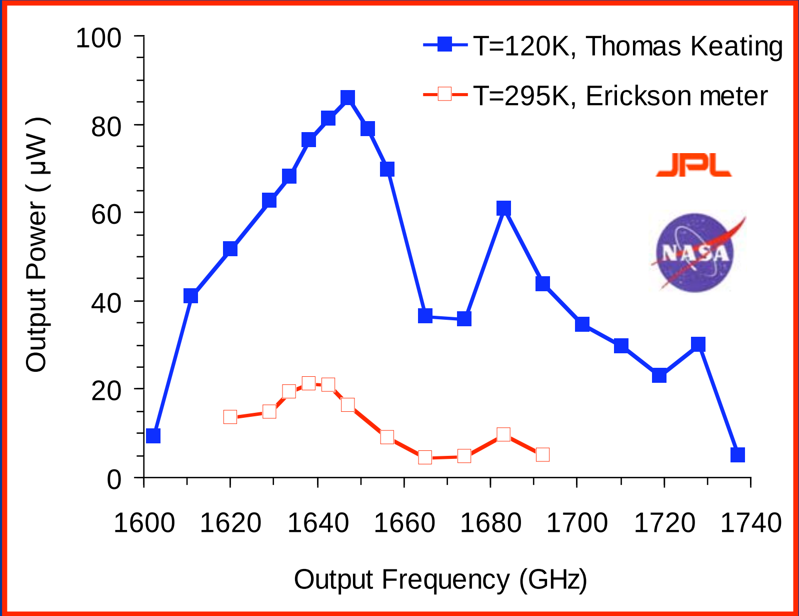
1.9THz balanced tripler biasless

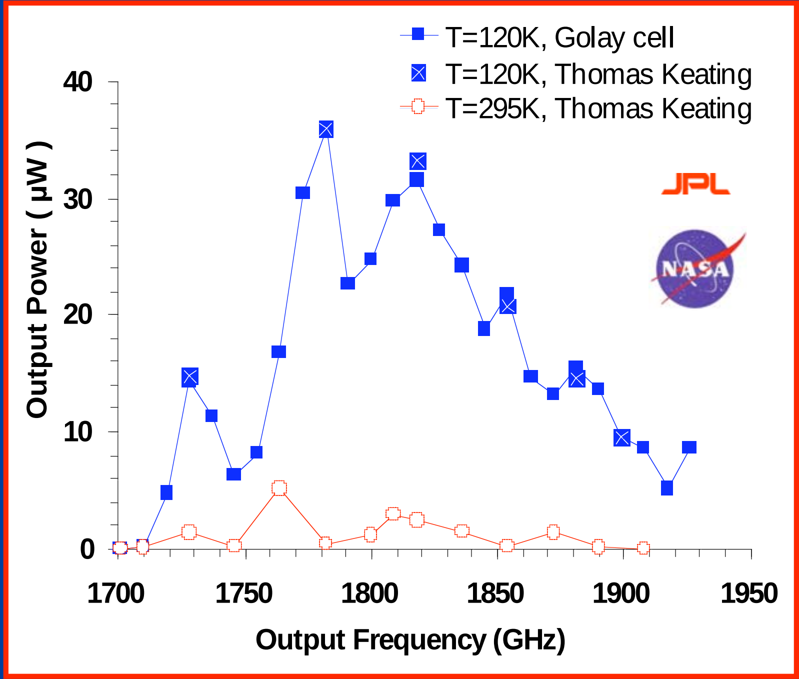
(detail of the diode area)



JPL 1.55-1.7 THz and 1.7-1.9 THz Balanced Triplers







Conclusions

- ✓ Diode-based MMIC-like circuit in waveguide mount gives the best performance in terms of power and bandwidth at sub-millimeter wavelength.

- ✓ Power and bandwidth of multiplier chains working in the 1 to 2 THz range is strongly limited by the power available in the 300-400GHz range

- ✓ Number of anode per chip is limited: increase in performance will come from advanced power combining schemes.

References

1. P. Penfield, R.P. Rafuse, *Varactor Applications*, Chapter 8: *Harmonic Multipliers*, MIT Press, 1962.
2. X. Mélique, A. Maestrini, P. Mounaix, M. Favreau, G. Beaudin, G. Goutoule, T. Närhi and D. Lippens, “Fabrication and performance of InP-based Heterostructure Barrier Varactors in a 250 GHz Waveguide Tripler”, *IEEE Trans. Microwave Theory Tech.*, Vol. 48, no. 6, pp 1000-1006, June 2000.
3. Alain Maestrini, John Ward, John Gill, Hamid Javadi, Erich Schlecht, Goutam Chattopadhyay, Frank Maiwald, Neal R. Erickson, and Imran Mehdi, “A 1.7 to 1.9 THz Local Oscillator Source”, in press, IEEE Microwave and Wireless Components Letters, Vol. 14, no. 6, June 2004.
4. A. Maestrini, J. Ward, J. Gill, H. Javadi, E. Schlecht, C. Tripon-Canseliet, G. Chattopadhyay and I. Mehdi, “A 540-640 GHz High Efficiency Four Anode Frequency Tripler,”, IEEE Transactions on Microwave Theory and Techniques, Vol. 53, pp. 2835–284, Sept. 2005.
5. T.W. Crowe, W.L. Bishop, W.L., D.W. Porterfield, J.L. Hesler, R.M. II Weikle, “Opening the THz window with integrated diode circuits”, IEEE Journal of Solid-State Circuits, Vol. 40, n°10, pp. 2104 - 2110, Oct. 2005.
6. Alain Maestrini, John S. Ward, Hamid Javadi, Charlotte Tripon-Canseliet, John Gill, Goutam Chattopadhyay, Erich Schlecht, and Imran Mehdi, “Local Oscillator Chain for 1.55 to 1.75 THz with 100 µW Peak Power”, IEEE Microwave and Wireless Component Letters, Vol. 15, Issue 12, pp. 871–873, Dec. 2005.