Broadband Sources in the 1-3 THz Range

Imran Mehdi[a], John Ward[b], Alain Maestrini[c], Goutam Chattopadhyay[a], Erich Schlecht[a], Bertrand Thomas[a], Robert Lin[a], Choonsup Lee[a], John Gill[a]
[a]Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA
[b]currently at Raytheon Co., Fort Wayne, Indiana, USA and [c]Université Pierre et Marie Curie – Paris

***Abstract*—Broadband electronically tunable sources in the terahertz range are a critical technology for enabling space-borne as well as ground-based applications. By power-combining MMIC amplifier and frequency tripler chips, we have recently demonstrated >1 mW of output power at 900 GHz. This source provides a stepping stone to enable sources in the 2-3 THz range that can sufficiently pump multi-pixel imaging arrays.**

I. Introduction and Background

Generation of coherent THz radiation remains a critical technological challenge for applications such as spectroscopy, imaging, communication and radar. Several recent articles have described the potential and capability of terahertz technology and how harnessing this technology can lead to exciting scientific discoveries in various fields (see [1] and references within). However, applications such as transmitters or heterodyne detectors would be difficult to realize without the development of suitable terahertz sources. A number of technologies exist that can provide terahertz radiation. While the output power of the source is often the single most important criterion for selecting the appropriate technology, from a systems point of view there are other criteria such as instantaneous bandwidth, DC-to-RF conversion efficiency, compactness, and spectral purity that can dictate the use of any particular technology.

In the last several years considerable progress has been made in understanding and more importantly being able to realize frequency multiplier chips that can produce useful amount of power in the terahertz range. However, as the operating frequency is increased, the output power decreases substantially and only a few microwatts of power have been demonstrated at 2 THz. This paper will discuss how power combining techniques have been utilized to substantially increase output power in the 1 THz range, which will in turn enable more powerful sources in the 2-3 THz range.

II. Technical Approach

One approach to achieving useful levels of output power in the 1-3 THz range is based on the straight-forward concept of power combining. Using this approach, the input stages of a cascaded chain of frequency multipliers are power-combined to produce enough power to drive succeeding stages. Millimeter-wave power amplifier technology is advancing rapidly, and it is expected that MMIC amplifiers based on GaN transistors will soon be available that produce several watts of continuous-wave power at frequencies above 100 GHz [2]. Even before these next-generation chips become available, power combining is already a proven method to increase amplifier power. For example, 0.8 W at 92.5 GHz from a W-band power amplifier module based on four power amplifier MMICs has already been demonstrated [3]. Future frequency multipliers will increasingly emphasize power handling as the dominant characteristic so long as multiplier output power is maximized.

Thermal heating, along with reverse breakdown can both limit a multiplier's power handling capability. To improve thermal design of multiplier chips an approach based on utilizing diamond substrates has been previously reported [4]. The second limitation to frequency multiplier power-handling occurs when the input signal to the multiplier becomes large enough to drive the diodes into reverse breakdown. Increasing anode area, increasing the number of anodes per chip, re-optimising doping levels, and moving to a high thermal conductivity substrate or GaN [5] will allow additional improvements in single-chip power handling. Once these possibilities have been fully exploited then power combining can further increase output power. Moreover, power combining allows one to use existing device designs and allows for a relatively simple path towards increasing output power.

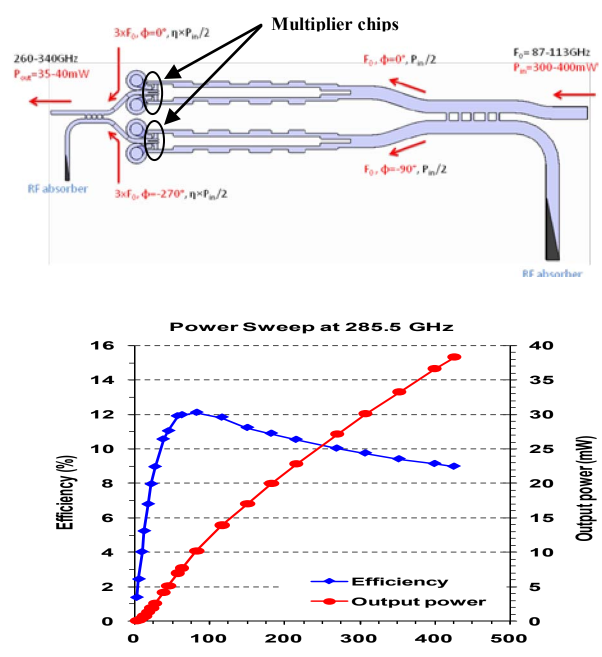

Figure 1: A 300 GHz tripler design based on power combining 4 chips is shown in the top half. Measured results from the tripler are shown in the bottom plot.

978-1-4244-5417-4/09/$26.00

III. RESULTS AND DISCUSSION

A two-chip in-phase power-combined frequency tripler working around 300 GHz has been demonstrated [6]. In this paper we report on a 4-chip design for a tripler working in the 260 to 340 GHz range. Figure 1 (top part) shows the schematic for this tripler circuit. It utilizes four identical chips with twenty-four anodes. This design also uses branchline quadrature hybrid couplers and internal loads to provide good return loss and isolation at both the input and output.

Despite the high frequencies involved and large fractional bandwidth, the power combining is nearly ideal, with the power-combined version performing with almost identical bandwidth and conversion efficiency as the single-circuit version except with four-times the power handling. The conversion efficiency of the power-combined tripler exceeds 10% for input powers ranging from 1.4 mW to 17 mW per anode with 24 anodes. The peak efficiency reaches a record 12% at 285.5 GHz and is obtained with around 100 mW of input power. With around 400 mW of input power the efficiency degrades to around 9%. This can be attributed to chip heating. The high efficiency over a large dynamic range makes this power-combined frequency tripler very versatile.

The power combined tripler sources can be used to drive higher frequency multipliers. Four-way power-combined amplifiers and the four-chip 300 GHz first stage multipliers have now been demonstrated. Work on the second stage 2-chip tripler and the final stage 2700 GHz tripler is currently underway.

As a preliminary step, we have pumped a single-chip 900 GHz tripler with the power-combined 300 GHz stage. For this experiment, it was sufficient to use the 2-chip power combined 300 GHz tripler. The dual-chip 300 GHz tripler and the single chip 900 GHz tripler (shown in Figure 2) have been previously detailed [6,7]. The x3x3 chain was operated at room temperature and also cooled to 77 K. The results from this experiment are shown in Figure 3. The power combining scheme allows us to obtain these power levels without compromising the device lifetime, even with a high power drive stage (typically 200 mW at W-band and 20 mW at 300 GHz). Thus, it is now possible to achieve 1.2 mW of output power above 900 GHz. However, an input power vs. output power characterization of the 900 GHz tripler indicates that the chip is getting saturated around 20 mW of input power. Thus, performance of this chain can be improved by utilizing power combining at 900 GHz. Such work is currently in progress. Once the 2-chip 900 GHz tripler is assembled and tested, we expect to demonstrate around 2 mW of output power.

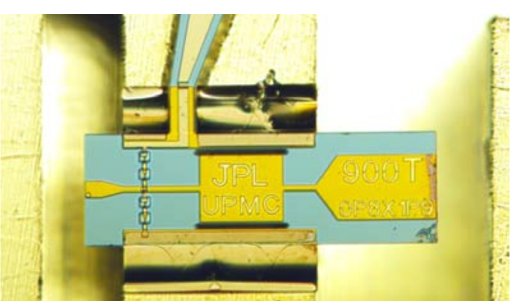

Figure 2: A four-anode 900 GHz tripler chip mounted in the bottom half of a split waveguide block.

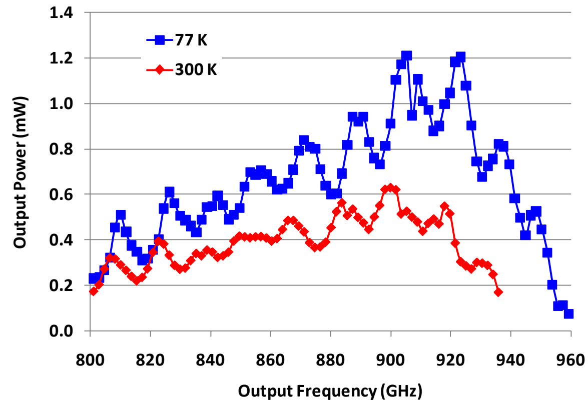

Figure 3: Performance of a x3x3 chain at room and cryogenic temperatures. A two-chip input-stage tripler was utilized to pump the output-stage single chip tripler.

IV. CONCLUSION

Multi-chip in-phase power combining techniques that use existing chips have been demonstrated. A substantial increase in output power at 1 THz based on this approach can in turn enable more powerful sources in the 2-3 THz range.

ACKNOWLEDGMENT

The research described herein was carried out at the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California, USA, under contract with the National Aeronautics and Space Administration.

REFERENCES

[1] P.H. Siegel, "Terahertz Technology," IEEE Trans. Microwave Theory Tech., Vol. 50, no. 3, March 2002.

[2] M. Micovic, A. Kurdoghlian, P. Hashimoto, M. Hu, M. Antcliffe, P. J. Willadsen, W. S. Wong, R. Bowen, I. Milosavljevic, A. Schmitz, M. Wetzel, and D. H. Chow, "GaN HFET for W-band Power Applications," International Electron Devices Meeting IEDM '06, pp. 1-3, Dec. 2006.

[3] John Ward, Goutam Chattopadhyay, John Gill, Hamid Javadi, Choonsup Lee, Robert Lin, Alain Maestrini, Frank Maiwald, Imran Mehdi, Erich Schlecht, and Peter Siegel "Tunable Broadband Frequency-Multiplied Terahertz Sources," (Invited Keynote), Proceedings, 33rd International Conference on Infrared, Millimeter, and Terahertz Waves, Pasadena, California, September 2008.

[4] Choonsup Lee, John Ward, Robert Lin, Erich Schlecht, G. Chattopadhyay, John Gill, Bertrand Thomas, A. Maestrini, Imran Mehdi, Peter Siegel, "A Wafer-Level Diamond Bonding Process To Improve Power Handling Capability of Submillimeter-wave Schottky Diode Multipliers," Proceedings of the 2009 International Microwave Symposium, Boston, June 2009.

[5] J.V. Siles and J. Grajal, "Capabilities of GaN Schottky Multipliers for LO Power Generation at Millimeter-Wave Bands," Proceedings, 19th International Symposium on Space Terahertz Technology, Groningen, April 2008.

[6] Alain Maestrini, John S. Ward, Charlotte Tripon-Canseliet, John J. Gill, Choonsup Lee, Hamid Javadi, Goutam Chattopadhyay, and Imran Mehdi, "In-Phase Power-Combined Frequency Triplers at 300 GHz," IEEE Microwave and Wireless Components Letters, Vol. 18, No. 3, March 2008.

[7] Alain Maestrini, John Ward, Goutam Chattopadhyay, Erich Schlecht, John Gill, Choonsup Lee, Hamid Javadi, and Imran Mehdi, "In-Phase Power Combining of Submillimeter-Wave Multipliers," (Invited) Proceedings, 33rd International Conference on Infrared, Millimeter, and Terahertz Waves, Pasadena, California, September 2008.