Single-Waveguide Power-Combined Multipliers for Next Generation LO Sources Above 100 GHz

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Abstract— **The next generation of local oscillator terahertz sources will demand novel and efficient power-combined frequency multiplier structures able to handle the increasing available power provided by state-of-the-art solid-state sources and amplifiers at W-band. In this paper, we give a brief overview of the different proposed alternatives and describe a new concept of frequency multiplier featuring two GaAs Schottky diode based MMIC chips on a single wave-guide structure. This scheme adds an extra symmetry to the multiplier circuit with respect to previously reported power-combined structures, increasing the power handling capabilities of frequency multipliers by an additional factor of two. GaAs foundry, post-processing, wave-guide block micromachining and testing will be fully performed within the European Union.**

I. INTRODUCTION

The use of power-combined Schottky multipliers will be essential for the next generation of multiplied local oscillator (LO) sources at submillimetre wavelengths in order to increase the available LO power at terahertz frequencies by taking advantage of the high power already available from driver amplifiers (up to 500 mW in the 70-113 GHz band) and of the several watts expected at W-band from MMIC amplifiers based on power-combined GaN transistors [1, 2].

The current generation of terahertz LO sources was designed and optimized considering a 100-150 mW LO power at W-band, featuring up to six Schottky anodes on a single multiplication stage. The required number of anodes is determined by the power-handling capabilities of a single Schottky diode, which is limited by forward conduction and reverse-breakdown effects and by the maximum sustainable power in order to avoid burnout problems [3, 4]. Since numerous constraints, e.g. the limited dimension of the transmission waveguide, make it difficult to design multipliers with many anodes without compromising the conversion efficiency and bandwidth [5], new approaches have to be employed in order to increase power-handling capabilities of traditional Schottky multipliers. Note that new frequency multiplier designs above 100 GHz will operate at input power levels one order of magnitude higher than the previous generation. Increasing anode areas, re-optimizing doping levels, employing high thermal conductivity substrates like diamond [6], and moving to GaN Schottky diodes for the lower frequency multiplication stages [7] will allow additional improvements in single-chip power-handling capabilities. Schemes consisting in using multi-gate Schottky diodes have also been proposed and demonstrated for increasing the number of anodes on a single multiplier.

Furthermore, strategies using several chips on a single split-waveguide multiplier block have been already reported in the literature with excellent results [8, 9]. These schemes consist of two or more mirror-image multiplier circuits that are power-combined in-phase in a single waveguide block using compact Y-junctions [8] and/or hybrid couplers [9, 10] at the input and output waveguides.

Here we describe the concept of a new power-combined multiplier consisting of a dual-chip single-waveguide topology that represents a further step in power-combined multipliers as it allows an increase in the power-handling capability by an additional factor of two. This is achieved by placing two symmetrical circuits directly into the same wave-guide transmission line. Moreover, this configuration might be used together with other power-combining schemes in order to obtain a record increase, by a factor of 4 (or more), in the power-handling capabilities of a single multiplier block.

This work is part of a European Space Agency (ESA) programme (ITT AO/1-5084/06/NL/GL) to investigate the potential for producing high quality submillimeter-wave mixer and multiplier circuits up to 380 GHz, through a combination of GaAs foundry-based device fabrication at United Monolithic Semiconductors and in-house post-processing of the device wafers [11].

II. POWER-COMBINED MULTIPLIERS FOR THE NEXT GENERATION OF LO SOURCES ABOVE 100 GHZ

Table I summarizes the measured output power from different Schottky diode-based multiplied LO chains up to terahertz frequencies consisting of single-chip frequency

multipliers (results from power-combined multipliers have not been included) [5, 12-18]. Most of these multipliers were designed by the Jet Propulsion Laboratory (JPL), Pasadena, CA in the frame of the Herschel Project of the European Space Agency. Some multiplier circuits from Virginia Diodes Inc, Charlottesville, VA (VDI) are also included. These circuits were optimized and tested considering a 100-150 mW available input power at W-band. The number of anodes employed for of each multiplier circuit is as well specified in Table I.

TABLE I
STATE-OF-THE-ART SINGLE-CHIP SCHOTTKY MULTIPLIERS AT THZ FREQUENCIES (DATA FOR 1&2 FROM [12], 3 FROM [13], 4 FROM [14], 5 FROM [15], 6 TO 9 FROM [16], 10 FROM [17], 11 FROM [18] AND 12 & 13 FROM [5]).

Design	Year	P_{in}	Anodes	T=300K	
				Peak η	P_{out}
1. JPL 180-215 GHz doubler	2000	150 mW	6	27 %	40 mW
2. JPL 360-430 GHz doubler	2000	36 mW	4	22 %	8 mW
3. JPL 1.12-1.25 THz tripler	2001	6-7 mW	2	~ 1.6 %	110 µW
4. JPL 735-850 GHz doubler	2002	9 mW	2	10 %	1.1 mW
5. JPL 1-7-1.9 THz tripler	2003	1-3 mW	2	0.2 %	3 µW
6. JPL 176-198 GHz doubler	2004	100 mW	6	33.5 %	34 mW
7. JPL 352-396 GHz doubler	2004	~ 34 mW	4	20 %	7 mW
8. JPL 704-792 GHz doubler	2004	~ 6 mW	2	10.5 %	0.6 mW
9. JPL 1.4-1.6 THz doubler	2004	~ 0.4 mW	2	3.5 %	15 µW
10. JPL 540-640 GHz tripler	2005	0.9-1.8 mW	4	9 %	1.8 mW
11. JPL 1.55-1.75 THz tripler	2005	3-4.2 mW	4	---	21 µW
12. VDI 220-235 GHz tripler	2007	150 mW	6	16 %	23 mW
13. VDI 405-465 GHz tripler	2007	75 mW	4	12 %	9 mW

For the next generation LO sources above 100 GHz, the number of anodes must be augmented, especially in the lower frequency stages, in order to make it possible to handle more than 1 W of input power at W-band. For example, ten times more anodes would be necessary to handle 1.5 W at W-band without re-optimizing the diode characteristics like anode areas, doping concentration, etc. Anodes areas can also be enlarged to increase power-handling capabilities, but this will have an important impact on the achievable frequency bandwidth. In either case, there will be a trade-off between the required anode sizes and the number of anodes. As a rough estimation, four-to-eight times more anodes will be necessary for the next-generation Schottky multiplication stages in the 200 GHz - 1 THz range.

Figs. 1 and 2 shows the first successful schemes reported in the literature to increase the number of diodes on frequency multipliers using the straight-forward concept of power-combining [8-10]. In the former, a 300 GHz frequency tripler featuring two MMIC chips with six-anodes is reported (12 anodes in total). In the latter, a 300 GHz tripler with six-anodes on four MMIC chips is presented (24 anodes in total). In both cases, similar efficiencies and frequency bandwidths than those obtained from an equivalent single-chip tripler have been measured with an increase by a factor of two and four in the output power, respectively [8-10].

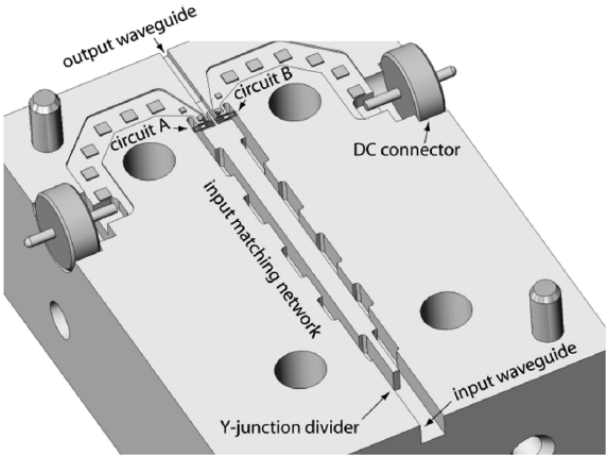

Fig. 1. 3-D schematic view of the bottom half of a dual-chip in-phase power-combined 260-340 GHz frequency tripler featuring Y-junctions (reprinted from [8]).

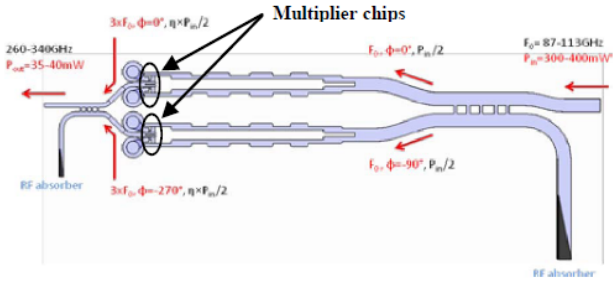

Fig. 2. Schematic view of a 300 GHz quad-chip in-phase power-combined frequency tripler featuring hybrid couplers and Y-junctions to divide/combine the input/output power before/after the Schottky diodes (reprinted from [10]).

An additional issue connected with high input power in frequency multiplier circuit design is the necessity to account for thermal issues in order to reduce the risk for burnout problems [3, 10]. The use of dual-gate Schottky diodes permits to increase the number of anodes on a single-chip by a factor of two, improving as well the thermal behaviour of the circuit [11]. This is illustrated in Fig. 3 for a 190 GHz Schottky diode-based frequency doubler designed at Rutherford Appleton Laboratory (RAL), Oxford, UK for the European Space Agency also under contract ITT AO/1-5084/06/NL/GL.

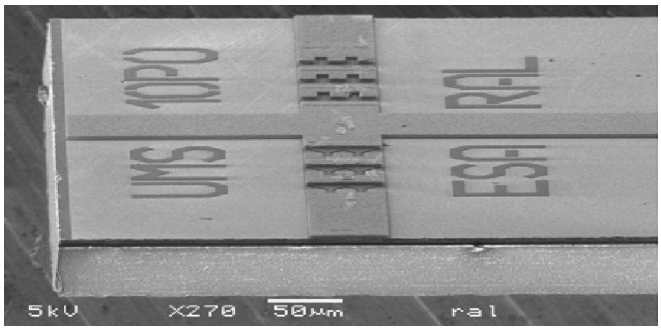

Fig. 3. SEM micrograph of a doubler circuit featuring six dual-gate Schottky diodes (reprinted from [11]).

The new power-combining topology described in this work defines a new symmetry plane within a split-waveguide block multiplier that allows to increase by an additional factor of two the number of anodes within frequency multipliers.

III. Dual-chip single-waveguide multiplier scheme

This dual-chip single-waveguide power-combining scheme consists of two chips symmetrically placed along the E-plane of the transmission waveguide, as shown in Fig. 4. Thus, the number of anodes that can be placed in a single-waveguide is doubled. To maximize the input power coupled to the diodes, the distance between the chips must be as short as possible, so they are located near the centre of the waveguide, coinciding with the maximum of the exciting TE_{10} mode.

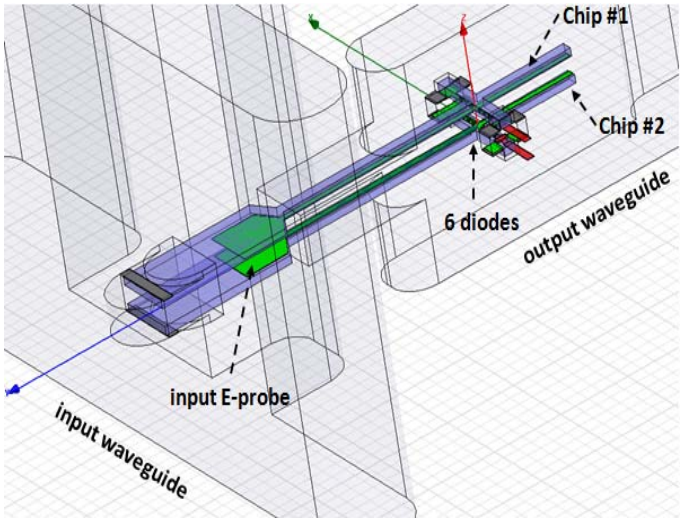

Fig. 4. Dual-chip single-waveguide power-combined scheme for multipliers.

The key advantage of this structure lies in its simplicity since the in-phase power-combining is carried out within a single transmission waveguide, without increasing the size of the circuit. Unlike other power-combining approaches, it is not necessary to duplicate the input and output matching networks and no hybrid couplers nor Y-junctions are required.

IV. A 190 GHz single-waveguide power-combined GaAs Schottky diode frequency doubler

To exemplify this concept, a 190 GHz frequency doubler based on this concept is presented. The doubler features two MMIC chips with a series array of 6 planar Schottky diodes each, integrated into a 50-µm-thick GaAs substrate. A bias-less design was chosen to accommodate the mixer-optimized UMS BES Schottky diodes that feature short epilayers and subsequently relatively low breakdown voltages. These two symmetrical circuits incorporate beam-leads to provide ground connections and a cross-shape substrate for lowering the dielectric load. This version of the doubler requires several post processing steps after the completion of the nominal UMS BES process. These steps are performed at the University of Bath and at RAL.

An alternative 190 GHz doubler design has already been made in the frame of this project and is now under fabrication. This alternative design is compact, biasless, tuneless and does not necessitate any post-processing steps (rectangular substrates are employed and no beam-leads are required). Thus, circuit repeatability is improved. These results will be presented in a future publication.

A. Design Process

The design methodology combines Agilent's Advanced Design System (ADS) linear / nonlinear harmonic balance circuit simulation to optimise the performance of the circuit, with Ansoft's High Frequency Structure Simulator (HFSS) 3-D electromagnetic simulation to model accurately the diodes geometry and waveguide structures. A custom symbolic defined device (SDD) model has been employed in ADS simulations in order to correctly model the physical response of UMS diodes. This model has been fitted using on-chip measurements of the I-V, C-V and resistance curves of the UMS diodes employed for the design. The measured electrical characteristics of these diodes are: an ideality factor of 1.17, a saturation current of $4 \cdot 10^{-14}$A, a series resistance of 4.4 Ω and a breakdown voltage lower than -5 V. It is important to remark that the UMS diodes are primarily intended for millimetre-wave MMIC mixers and are not optimum for use as frequency multipliers.

B. Post-Processing

The foundry-fabricated wafer tiles are then post-processed both to pattern and separate the circuit structures and to form the beam-leads used to provide accurate RF grounding. The wafer tiles are first pattern and etched from the top-side to delineate the individual circuit chip outlines. This is achieved via reactive-ion or inductively-coupled plasma etching (RIE / ICP) through the passivation and GaAs layers down to a depth of around 70µm. The wafer tiles are then glued face-down on to a carrier wafer and mechanically lapped to a substrate thickness of 50µm, revealing the back surfaces of the circuit structures. Back-side lithography is the used to provide an RIE/ICP etch mask defining the final circuit chip shapes. The wafer tiles are RIE/ICP etched through the top-side, removing the unwanted material under the beam-leads in the process. Finally, the glue is dissolved to release the individual circuit structures from the carrier wafer.

C. Expected results

A ~10 % efficiency over a 15 % 3-dB bandwidth is expected for the 190 GHz doubler when pumped with 80 mW, according to circuit simulations shown in Fig. 5. The MMIC chips have been delivered by UMS and post-processed at the University of Bath, UK. The multiplier blocks are being fabricated at RAL, Oxford, UK (see Fig. 6). Although the multiplier was optimised for operation at a bias voltage of zero volts, two separate bias paths have been included in the circuit to mitigate possible mismatches. RF measurements are planned for the summer of 2010.

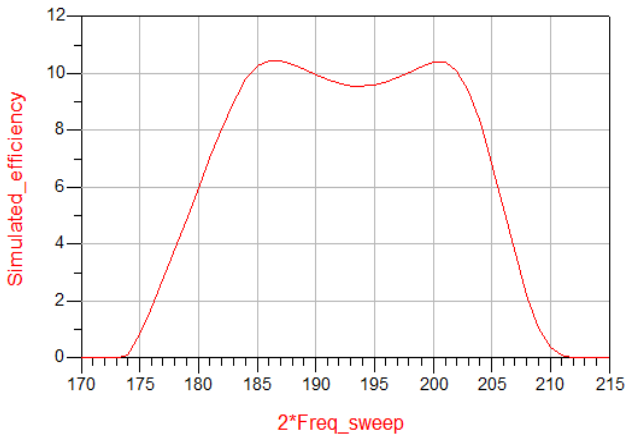

Fig. 5. Simulated efficiency of the 190 GHz dual-chip Schottky doubler for an 80mW constant input power.

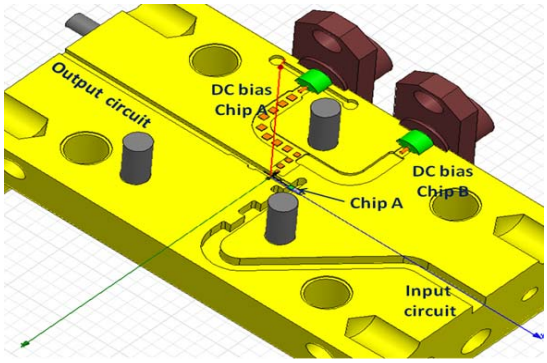

Fig. 6. 190 GHz dual-chip single-waveguide doubler block (bottom part).

V. Conclusions

A 190 GHz power-combined frequency doubler featuring two MMICs in a single waveguide structure has been fabricated using Schottky diodes from UMS-BES foundry process combined with additional post-processing processes performed at the University of Bath and at RAL. Although state-of-the-art efficiency is not expected since not optimum diodes for multiplier operation have been employed, this novel multiplier scheme is believed to have the potential to greatly enhance the output power delivered by frequency multipliers at submillimetre-wave frequencies.

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