A 5mW-290 GHz HETEROSTRUCTURE BARRIER TRIPLER IN A WAVEGUIDE CONFIGURATION

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ABSTRACT

An output power of 5 mW has been demonstrated at 290 GHz by tripling a primary signal in the W band. The non-linear devices are high performance InP-based Heterostructure Barrier Varactors mounted in a mechanically tuned waveguide harmonic multiplier. The flange-to-flange maximum efficiency was 5 % whereas the bandwidth is around 30 GHz. These results are the highest to date for an HBV multiplier operating at these frequencies.

I. INTRODUCTION

HBV multipliers tend now to compete with their Schottky varactor counterparts in the millimeter wave spectrum [1]-[8]. We demonstrated at 247 GHz record performances, with discrete devices (9.6 mW with 11.5 % maximum efficiency) [3] whereas improved results (13.5%, P_{out}> 10 mW) were published recently at 210 GHz [8]. Also, at lower frequencies (~ 140 GHz), excellent performances have been pointed out using a non-linear transmission line approach [7] and array configuration [6]. The basic reason for these performances is the natural symmetry of the non-linear C-V characteristic around zero-volt, afforded by the use of non-rectifying contacts. Such a symmetry dramatically improves the functionality of the devices by avoiding the introduction of idler circuits for a tripling operation. Another key advantage stems from the possibility of stacking several barriers, thus avoiding the necessity of a multiple mesa configuration. By a proper design of the epilayers, the capacitance of the device along with the voltage (power) handling can thus be tailored. Under these conditions, some improvements in the frequency capability of the devices, with simultaneously the supply of an output power in the milliwatt range, can be expected. In this communication, we analyze such a possibility with operation frequencies ranging between 275 GHz and 320 GHz. In practice, the highest performance was obtained at 290 GHz with 5.7 mW power. In addition, the operating bandwidth is relatively broad, a welcome feature for most applications. In section II, we report on the device fabrication of the non-linear devices, which are the key elements as described above. In section III, we discuss the small signal characteristics in terms of capacitance-voltage relationship, series resistance and parasitic interconnect elements. Section IV deals with the design of the multiplier block. Finally, the large signal characteristics are reported in section V.

II. DEVICE FABRICATION

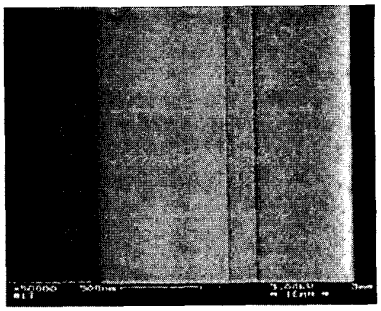

Figure 1: Scanning Electron Micrograph of dual barriers integrated during the epitaxial growth.

The device fabrication made use of an InP-based technology. Basically, this choice was dictated by the necessity of an efficient heterostructure blocking barrier, which was achieved due to a tri-layered 5nm-InAlAs/3nm-AlAs/5nm-InAlAs barrier scheme (Fig. 1). The Indium concentration ($In_{0.52}Al_{0.48}As$) corresponds to lattice-matched conditions to the InP substrate whereas the AlAs epilayer was pseudomorphically grown by gas source molecular beam epitaxy. The capacitance

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modulation takes place in the cladding layers via the accumulation process at the hetero-interface. For this study we have varied the cladding layer doping concentration in the 1-2x10 ^{17} cm^{-3} range. By these means, the current capability of the device is sufficient to cope with the very large displacement current at the targeted frequency, under hard pumping conditions. Special attention was also paid to the contact layers with doping concentration in the 5x10^{18}-1x10^{19}cm^{-3} region, in order to minimize, as far as possible, the series resistance.

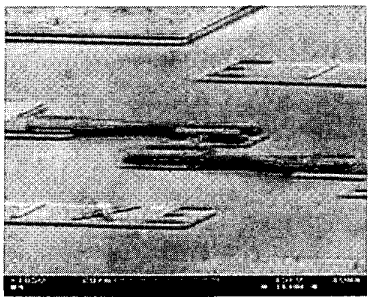

Figure 2 : SEM of an air bridge contacted HBV device.

The device fabrication involves (i) the electron beam writing of the active area, followed by ohmic contact material evaporation, (ii) the etching of the mesa by Reactive Ion Etching, (iii) the implementation of side ohmic contacts, (iv) the fabrication of air-bridge interconnects by gold evaporation or electroplating. Figure 2 shows a SEM of a typical device, which involves epitaxial stacking and planar integration.

III. SMALL SIGNAL CHARACTERIZATION

The small signal characterization consists in extensive measurements of the scattering parameters of devices, which can be characterized by wafer probing in the 50 MHz-110 GHz frequency range. The intrinsic elements were directly measured from large area samples, so that the diode lumped elements can be deduced without the need of de-embedding techniques. The parasitic interconnects were also treated as lumped elements and have been determined by a close fit between the frequency dependence of the diode reflection coefficient, which was measured and calculated respectively. Also, a two-tip wafer probing measurement was carried out on the microstrip type samples, intended to be mounted in the multiplier block. Figure 3 shows the conductance-voltage characteristic of a typical device, with an area of ~300 μm^2, which integrates two barriers in series.

At a voltage of 8 V, a significant conduction takes place (4 V for a single barrier device). This is in agreement with theoretical calculations of conduction characteristics through tunneling leakage currents.

The capacitance characteristic for the same epitaxial parameters is also reported in Fig. 3. The zero-bias capacitance was ~1.7 fF/μm^2 (two barriers) for a capacitance ratio of about 4:1. It is also worth mentioning that an excellent symmetry in the C(V) curve was achieved so that the even harmonics are rejected in multiplication experiments. In the present technological batch, fabricated on a semiconductor substrate, the parasitic capacitance was found in the 20 fF range, due to the relatively high value of the pad-to-pad capacitance. The self inductance was typically in the 50-75 pH range. The series resistance, with a dominant contribution by the spreading resistance, was a few ohms depending of the device area.

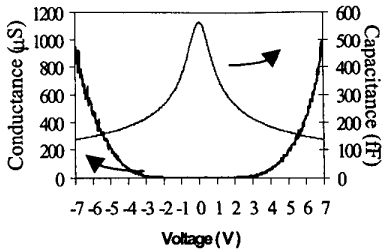

Figure 3: conductance and capacitance voltage characteristics of a typical HBV device (two barriers in series , Nd= 2x 10 ^{17} cm^{-3})

IV. MULTIPLIER BLOCK

The multiplier is a cross waveguide test fixture interconnected by a micro-strip type transmission line onto which the radiating, filtering and matching elements can be implemented in a MMIC-like fashion. Their design was performed by means of electromagnetic simulations using HFSS code by HP. Figure 4 thus shows the 3-D view of output section of the multiplier mount. The input waveguide was WR 10 (75-110GHz) and the output waveguide was WR3 (220-325 GHz).

In a first stage, the scattering elements of each circuit were calculated separately for optimization. The simulation of the multiplier, taken as a whole, was carried out using circuit ADS code. In order to illustrate such a procedure, we plotted in Figure 4 the electric field pattern in two orthogonal planes. A low pass filter was placed in the input section. The substrate was a low refractive index 75 μm-thick quartz wafer embedded in a rectangular-type cavity. The simulations were also performed in 3-D and thus takes into account the influence of the shielding.

An EM transition, matched by sliding shorts performs the mode matching between the input waveguide and the strip circuit. It was an E-plane suspended strip on quartz. Its optimization (insertion loss and bandwidth) can be carried out independently with two back-to-back schemes.

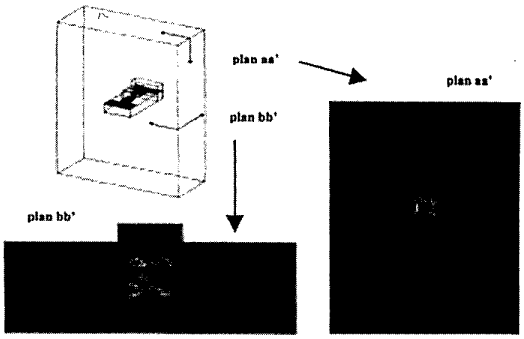

Figure 4: electromagnetic simulation of the output section.

In practice, several device areas (between 10 and 50 μm^2) are available on the mask set, with the aim to study the diode behavior under broad band conditions. For the matching, we decided to use a mixed technique with conventional mechanically tuned E-H plane backshorts in the output section and adjustable stub-like elements placed in close proximity to the diode. The optimized impedances of the load and source were estimated after fitting the C(V) experimental characteristics and subsequent harmonic balance simulations. Figure 5 is a photo of the corresponding block, which was fabricated for this project.

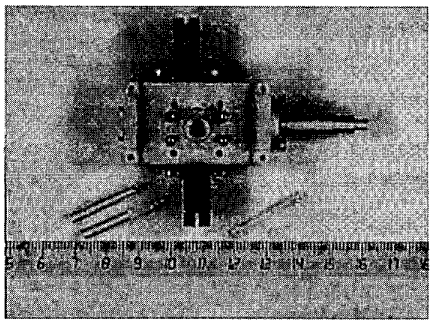

Figure 5 : photograph of the test fixture.

V. LARGE SIGNAL EXPERIMENT

Prior to the mounting in the multiplier block, the samples were pre-diced on the top surface. Subsequently, the rear side of the substrate was lapped. By this way, it is possible to alleviate leakage substrate modes promoted by the high permittivity of the semiconductor. The samples are then cleaved into discrete chips with the following typical dimensions 200x100x50 μm^3. Ideally, thinner wafers would be more suitable but this introduces handling problems. Recently, we have increased our yield by pre-dicing, using precision-sawing/wafer thinning techniques. We have also investigated the possibility of pre-scribing by means of surface micromachining using wet chemical etching in order to achieve even higher yields.

The experimental set up consists of a carcinotron, which can be tuned at W-band with a relatively high output power. The up-converted power was measured by means of an *Anritsu* power meter, which has been previously calibrated using a *Thomas Keating* power meter. Figure 6 shows a view of the experimental setup. Also, some network analysis can be performed using an AB millimeter set up.

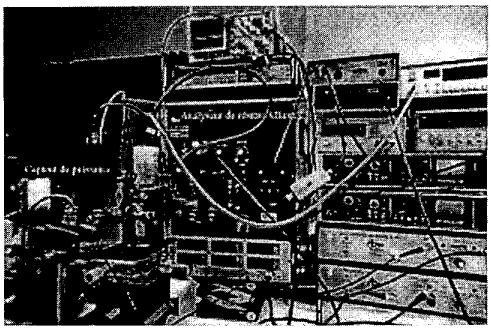

Figure 6 : photograph of the experimental set up.

The discrete devices have been mounted in a flip-chip configuration by soldering them onto two pads, which cross the output waveguide, located on the quartz wafer.

Figure 7 shows the variations of the output power as a function of input frequency. The maximum power was achieved at 96.4 GHz (~290 GHz) with a maximum output power of about 5.7 mW. Also, It should be emphasized that the 3 dB band extends from 92 GHz to 103.5 GHz by taking a 5 mW as a reference. This means that a significant amount of power can be up-converted in a 30 GHz bandwidth provided a fine tuning can be carried out.

The input power delivered by the pump source was in the 100 mW range. A flange-to flange efficiency of ~5 % was thus obtained. To our knowledge, these are the best results published, notably in terms of the output power, for HBV device technology at these frequencies. Such a result also compares with the state-of-the art results of Schottky-varactor devices established in reference [9].
The variation of the output power as a function of input power recorded at 290 GHz shows a dramatic increase in the up-converted power for an input power in excess of 20 mW. The maximum efficiency was obtained for typically 60 mW input power.

We are currently investigating the origin of the broadband operation, which depends primarily on the sensitivity of the optimal source and load impedances as a function of frequency. However, experimentally, it can be noted that the multiplier performance was highly dependent on the related circuitry. Notably the quasi-

lumped matching circuit shows a large influence on the overall performance. The other dominant contribution is the mechanical tolerance of the test fixture, e.g. those of the sliding shorts. Some improvement towards a very broadband multiplier can be foreseen in a more monolithic circuit approach.

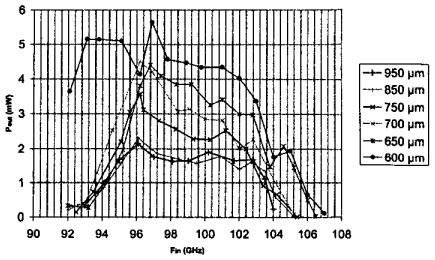

Figure 7 : variations versus frequency of the up-converted power

VI. CONCLUSION

A record performance has been demonstrated for a HBV multiplier operating between 276 and 318 GHz. The measured devices exhibit highly symmetrical C-V characteristics with a capacitance ratio as high as 4:1 and a voltage handling in the 4 V range for a single device. A maximum output power, close to 6 mW, was achieved at 290 GHz along with a 30 % bandwidth taken 5 mW as a reference. It is believed that further improvement can be achieved using the Buried Metal Technology (BML), which was demonstrated in our group following the lift-off and transfer of the devices on quartz [10].

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