

# A Broadband 900-GHz Silicon Micromachined Two-Anode Frequency Tripler

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**Abstract**—The design, fabrication, and measurement are presented for a 900-GHz frequency tripler with silicon micromachined blocks made using deep reactive ion etching. The broadband design results in more than 60  $\mu\text{W}$  between 877.5–922.5 GHz and the peak output power of 85.3  $\mu\text{W}$  in the frequency response, all measured at room temperature. In power sweep measurement, the tripler delivers the maximum power of 109.3  $\mu\text{W}$  at 909 GHz. This is the first demonstration of a frequency tripler using silicon micromachining at these frequencies and suggests that this technology is a viable option for receiver arrays in the terahertz frequency range.

**Index Terms**—Balanced diodes, frequency multiplier, micromachining, Schottky diode, submillimeter wave.

## I. INTRODUCTION

TERAHERTZ sources have attracted recent interest for both terrestrial and astronomical applications [1], [2]. The abundant terahertz radiation in our universe contains a wealth of scientific information. A superheterodyne radiometer is an important instrument for conducting quantitative spectroscopy on space missions. For such applications, it is important to have compact sources that produce enough power to pump the receiver mixers, but are also broadband and can be implemented in multipixel receiver arrays of the future.

Tube-type terahertz signal sources, including backward-wave oscillators, gyrotrons, and klystrons, have been used for decades [3], [4], but they are bulky and costly to build. The miniaturization of tube-type sources is being investigated using nanotube and micromachining techniques [5]. On the other hand, solid-state devices provide a compact and lightweight solution for the generation of terahertz radiation. Quantum cascade lasers [6] may play an important role in the generation of terahertz signals when the technology becomes mature. Although rapid advances

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have been made in amplifiers and two-terminal oscillators [7], especially high electron-mobility transistor (HEMT) [8], hetero-junction bipolar transistor (HBT) [9], and heterostructure barrier varactor (HBV) diodes [10]–[12], GaAs Schottky diodes still provide great performance advantage and are widely used in terahertz frequency multipliers [13], [14].

Planar Schottky diode chips are normally housed in a waveguide block that provides appropriate input and output matching conditions. Traditionally, metal machining [15] makes use of high precision lathes and milling machines to fabricate waveguide blocks for terahertz circuits, such as frequency multipliers [10], [16], power-combining circuits [17], [18], and corrugated horns [19]. However, metal machining becomes difficult as feature sizes decrease, and the cost may become prohibitive for multipixel receiver arrays.

Besides metal machining, other techniques have been proposed for terahertz waveguides, including electroforming, surface micromachining, stereolithography, laser beam etching, wet etching, and dry etching. Electroforming [20] is suitable for producing complex waveguide structures, but the process is slow and still requires machining of a high-precision mandrel.

Surface micromachining employs thick photoresist, such as SU-8, to build terahertz waveguide blocks [21], [22]. The fabrication of surface micromachining is relatively simple, but usually has a long baking and curing time [23]. Instead of using thick photoresist as structure layers, metal-film waveguides use thick photoresists as sacrificial layers [24]. The metal-film process is not suitable for building full-height waveguides due to the photoresist thickness limit. A reduced height waveguide horn antenna was reported in [25] at 200 GHz.

Unlike surface micromachining that uses the photo-definable polymer, a 3-D stereolithographic technique is to use laser beams to cure the resin layer by layer [26], [27]. Waveguide structures are immersed in resin, and the fabrication process is not compatible with the standard CMOS process. X-ray LIGA is a complex process, allowing to achieve structures with very high aspect ratio and deliver nearly perfect geometries [28], but, this process is expensive and requires a thick X-ray mask.

Without using photoresist or resin, laser beam etching has been proposed to etch silicon with the use of chemical reactions. The laser beam etching method is capable of producing complex 3-D structures, such as a 2-THz feedhorn [29]. This method is suitable for terahertz circuits because only 1–2- $\mu\text{m}$ -thick silicon is etched away as the laser beam moves.

Wet etching is simple and has been widely used in waveguides [30], filters [31], antennas [32], and mixers [33], but wet etching is limited by the crystal orientation of silicon wafers and

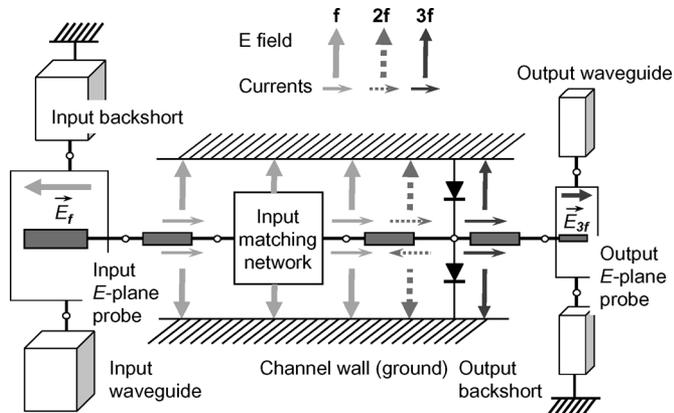


Fig. 1. Block diagram of a two-anode 900-GHz balanced tripler.  $\vec{E}_f$  and  $\vec{E}_{3f}$  stand, respectively, for the electric field at the fundamental frequency  $f$  and at the output frequency  $3f$ . The electric fields and the current lines are represented for the fundamental frequency  $f$  (thick light lines), idler frequency  $2f$  (dashed lines), and output frequency  $3f$  (light plain lines).

accurate dimensional control is also difficult. Deep reactive ion etching (DRIE) is a dry etching technique that is amenable to mass production, inherently suitable for high-precision design, and works with all types of silicon substrates. DRIE has been used for a wide range of millimeter-wave and submillimeter-wave waveguide circuits, including  $W$ -band circuits [34], [35] a 260-GHz tripler [36], a 325–500-GHz quadrature hybrid [37], and a 600-GHz mixer [38].

Previous triplers with demonstrated over 0.5-mW output power around 900 GHz were measured at cryogenic temperatures and also have the tripler chips with dc bias [39]. Similarly, a 900-GHz source, where the output power was the primary goal instead of the bandwidth, achieved over 2 mW using a power-combining technique and two four-anode tripler chips with dc bias when cooled to 120 K [40].

The proposed tripler has a two-anode chip without using dc bias and is measured at room temperature. In this paper, 16 silicon micromachined blocks were fabricated in parallel for the proposed 900-GHz tripler using a 4-in low-resistivity wafer. The broadband balanced 900-GHz silicon micromachined tripler is demonstrated for the first time. This paper is organized as follows. Section II introduces the circuit design. Section III describes the fabrication and assembly of the micromachined waveguides. The measurement and analysis are presented in Section IV, and a conclusion follows in Section V.

## II. CIRCUIT DESIGN

### A. Design Methodology

The topology of the 900-GHz tripler chip is shown in Fig. 1 and is based on the widely used antiparallel diode configuration [41]–[43] to cancel unwanted harmonics. The diodes of the tripler chip are in series at dc and are balanced at RF. The chip is mounted in an  $E$ -plane split block. Input signals are coupled to a suspended microstrip line by an  $E$ -plane probe on the chip's GaAs membrane, which supports the propagation in a quasi-TEM mode. A microstrip matching network, consisting of low- and high-impedance lines on the membrane, is employed to

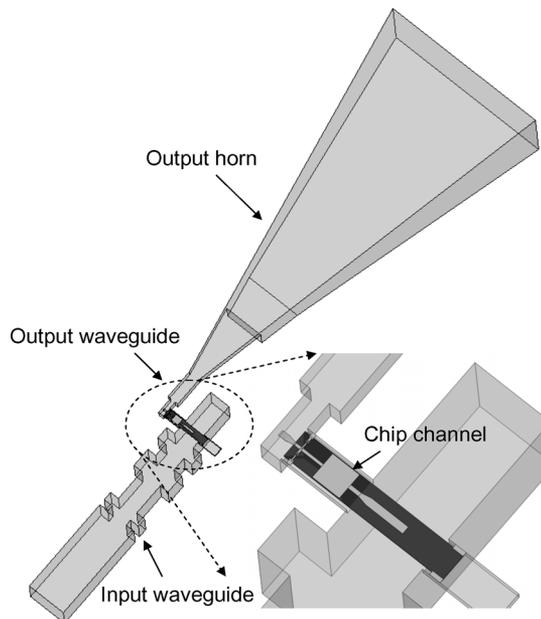


Fig. 2. Drawing of half of the 900-GHz frequency tripler. This tripler is a split-block waveguide design and has the waveguide structure cut along the  $E$ -plane center. The tripler structure, including input/output waveguides and chip channel, is made of silicon and released from a 4-in wafer. The tripler structure and tripler chip are then assembled and mounted on a fixture for measurement.

match the diodes at the input frequencies and used as a low-pass filter that helps prevent the third harmonic from leaking into the input waveguide. The third harmonic produced by the diodes is coupled to the output waveguide by the second  $E$ -plane probe on the same GaAs membrane. Metallic on-chip beamleads allow for the handling and mounting of the chip inside the waveguide block.

Passive circuits are first simulated using Ansoft HFSS. The extracted  $S$ -parameter files are imported into Agilent ADS, and the frequency tripler chip is optimized for output power and conversion efficiency. Fig. 2 depicts the bottom half of the tripler block with the tripler chip. The chip is fabricated on a thin GaAs membrane at the Jet Propulsion Laboratory (JPL), Pasadena, CA [44], and is simply dropped in the chip channel without the use of solder or epoxy. The simplicity of the design makes the assembly of the entire block relatively easy and repeatable.

### B. Waveguide Circuits Design

The waveguide circuits, including the chip channel and the input/output waveguides in Fig. 2, are designed to maximize the output power over a wide bandwidth, after the optimization of diodes [41]. The chip channel, housing the membrane chip between the input and output waveguides, cuts off the TE mode of the suspended microstrip line. Thus, only a quasi-TEM mode is allowed to propagate inside the channel at the input frequency. The third harmonic generated by the diodes propagates in the quasi-TEM mode in the chip channel and is coupled to the output waveguide through the second  $E$ -plane probe. The output waveguide has a cutoff frequency of 680 GHz and does not allow the propagation of the second harmonic.

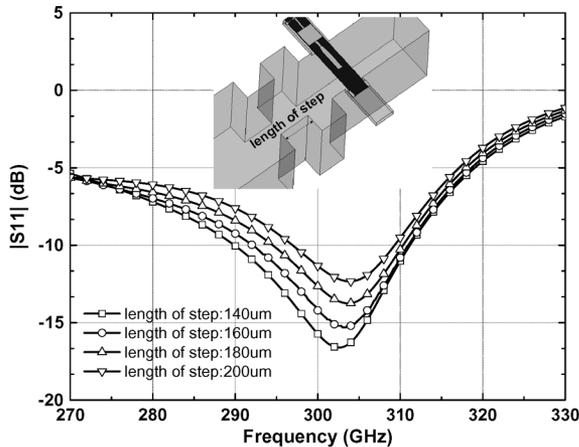


Fig. 3. 10-dB return-loss bandwidth versus the length of one capacitive step.

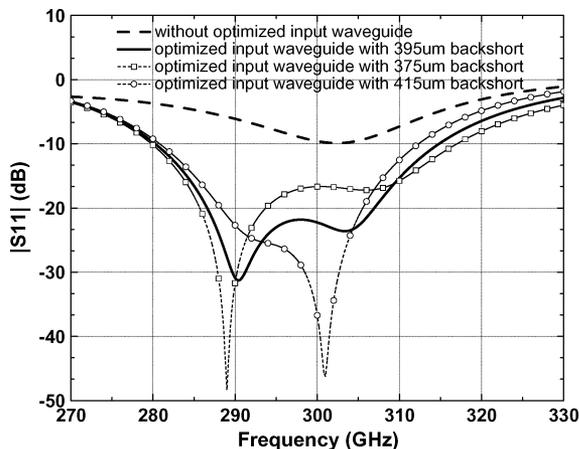
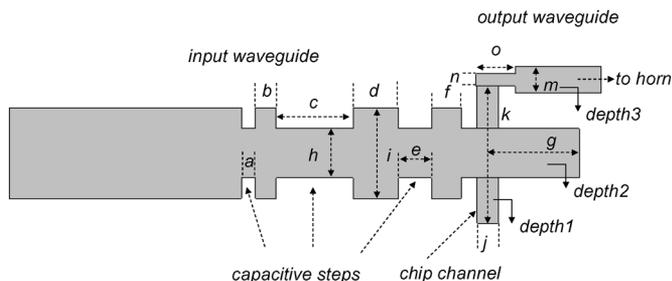

 Fig. 4. Input return loss in the harmonic-balance simulation with and without the optimized input waveguide. The input return loss with optimized input waveguide (solid line) shows improved 10-dB bandwidth compared to the simulation without optimized input waveguide (dashed line without a symbol). The optimized input backshort is 395  $\mu\text{m}$ . The on-chip matching network is included in all simulations.


Fig. 5. Optimized waveguide sections and chip channel. Horn antenna is not shown.

A theoretical model of the transition from a planar  $E$ -plane probe, which is extended part way across waveguide, to a rectangular waveguide was developed and the input impedance of a freestanding probe was defined by  $Z_{\text{in}} = R_{\text{in}} + jX_{\text{in}}$  [45]. The real part,  $R_{\text{in}}$ , depends only on the propagating mode of the first TE mode and the imaginary part,  $X_{\text{in}}$ , is approximately proportional to the change of waveguide height [46]. A reduced height waveguide is preferable for its reduced imaginary part

 TABLE I  
 DIMENSIONS OF THE INPUT WAVEGUIDES AND CHIP CHANNEL  
 (APPROXIMATE VALUES)

symbol	value ( $\mu\text{m}$ )	symbol	value ( $\mu\text{m}$ )
$a$	60	$b$	90
$c$	330	$d$	200
$e$	140	$f$	130
$g$	395	$h$	220
$i$	400	$j$	90
$k$	600	$m$	120
$n$	60	$o$	170
$depth1$	30	$depth2$	400
$depth3$	110		

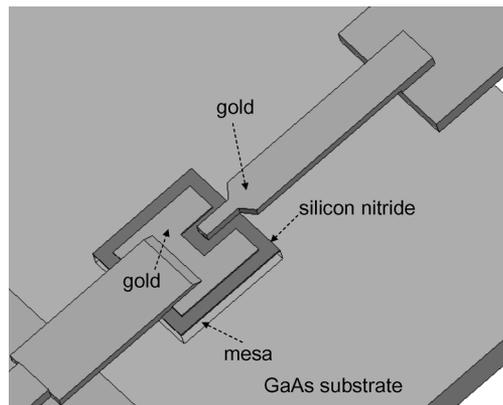


Fig. 6. Accurate 3-D model of the Schottky diode used in the full-wave simulation.

 TABLE II  
 PHYSICAL AND ELECTRICAL PARAMETERS OF THE  
 JPL 900-GHZ BALANCE TRIPLER

Physical and electrical parameters	
Anode width	0.4 $\mu\text{m}$
Anode length	1.4 $\mu\text{m}$
Epilayer doping	$5 \times 10^{17}$
GaAs thickness	3 $\mu\text{m}$
$C_j$	1.5 $fF$
$R_s$ at dc	35 $\Omega$

of the probe's impedance, especially when the micromachining technique is capable of delivering the reduced height structures.

An additional capacitive  $E$ -plane step in [46] was reported to increase the bandwidth of the transition with a radial probe. In our study, capacitive steps are used with the reduced height input waveguide and a rectangular probe to increase the bandwidth of input return loss in the harmonic-balance simulation, including the diodes, parasitics, and output waveguide. The reduced height of capacitive step is 220  $\mu\text{m}$  for tuning out the residual impedance variation of the probe [46]. Fig. 3 shows the optimization of 10-dB return-loss bandwidth by the length of only one capacitive step.

The number of capacitive steps and the length of each step are optimized until the desired return loss is obtained and the matching technique of capacitive  $E$ -plane steps in a rectangular waveguide is introduced in [47]. The optimized input waveguide

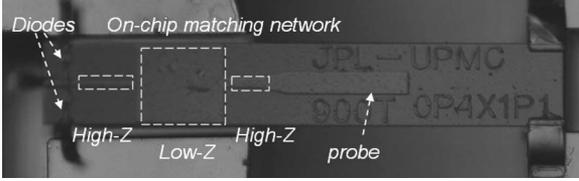


Fig. 7. On-chip matching network consists of high- and low-impedance microstrip lines between the *E*-plane probe and diodes.

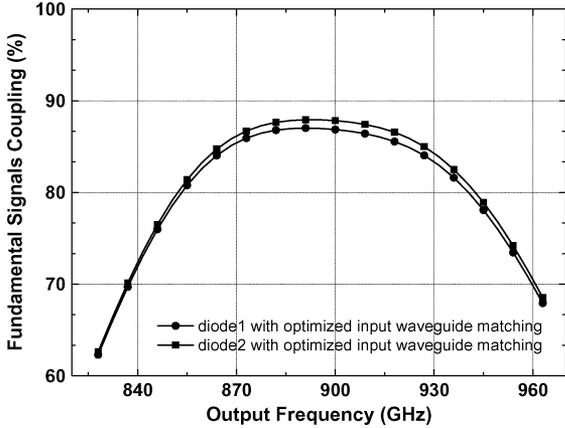


Fig. 8. Simulated input coupling per diode of the 900-GHz balanced triplers.

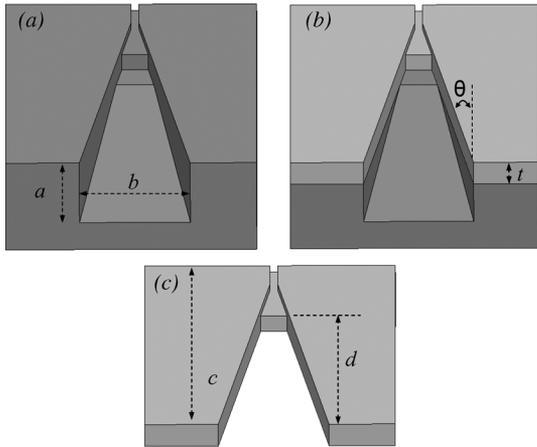


Fig. 9. Depiction of the micromachining process used to form the horn. (a) Half of the horn split along the *E*-plane center. (b) Silicon block on top of the fixture. (c) Silicon block only.

has three capacitive steps and the 10-dB return-loss bandwidth is increased to 34 GHz in the harmonic-balance simulation, as shown in Fig. 4 (solid line). The length of the input backshort is initially chosen to be a quarter wavelength at the fundamental frequency and the optimized length increases due to the capacitive steps. Fig. 4 shows the return loss of optimized input backshort (395- $\mu\text{m}$  long) and the backshort with the length of 375 and 415  $\mu\text{m}$ . The input waveguide port has the same cross section (800  $\mu\text{m} \times 400 \mu\text{m}$ ) as the output of a broadband 300-GHz tripler used to generate input signals. The output waveguide is designed in the same way as the input waveguide by maximizing the output power.

The optimized dimension of the input and output waveguide and the chip channel are provided in Fig. 5 and Table I. The opti-

TABLE III  
DIMENSIONS OF THE 900-GHz MICROMACHINED ANTENNA  
(APPROXIMATE VALUES)

Dimensions	Value ( $\mu\text{m}$ )
<i>a</i>	1100
<i>b</i>	1680
<i>c</i>	4320
<i>d</i>	3120
<i>t</i>	400
$\theta$	11.5°

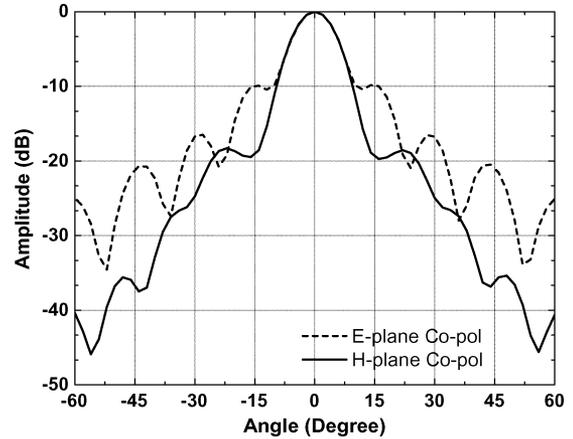


Fig. 10. Simulated far-field patterns of the 900-GHz micromachined horn.

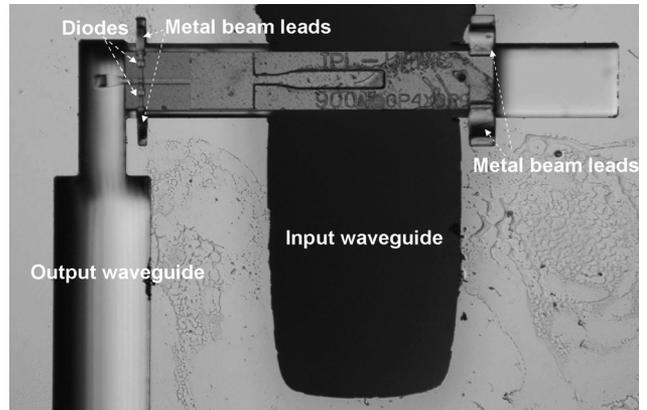


Fig. 11. Tripler chip in the micromachined waveguide structures. The metal beamleads on the terahertz chip greatly improve the chip handling and make the assembly highly repeatable.

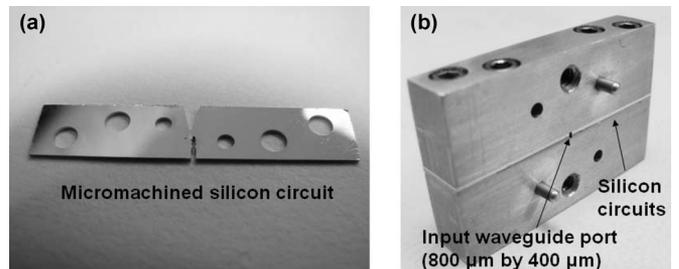


Fig. 12. Images of: (a) micromachined silicon circuit and (b) fixture with the silicon circuit and tripler chip.

mized input backshort is 395- $\mu\text{m}$  long, and the output backshort is 50- $\mu\text{m}$  long, all measured from the center of the tripler chip.

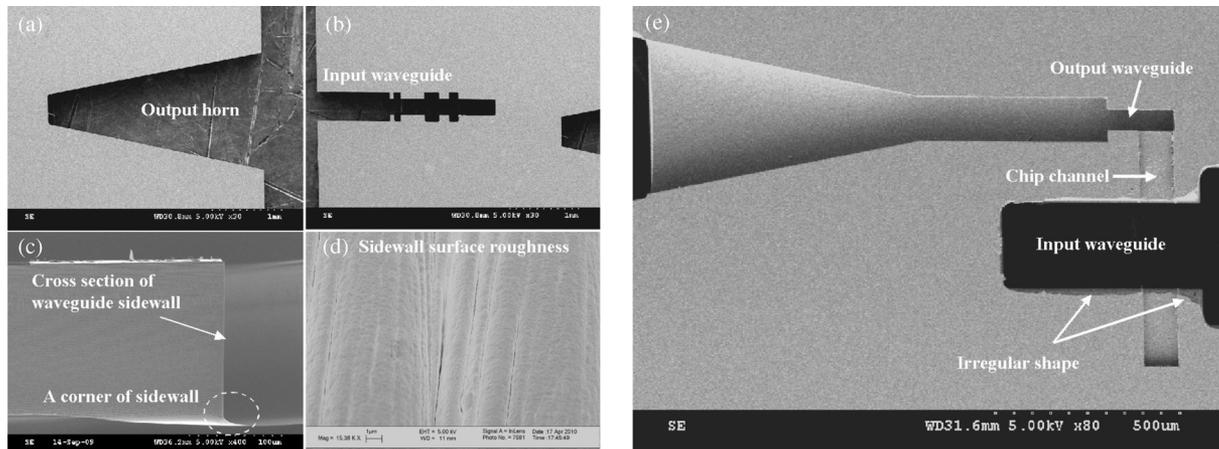


Fig. 13. SEM images. (a) Output horn. (b) Input waveguide. (c) Cross section of waveguide sidewall. (d) Surface roughness on sidewall. (e) Input and output backshorts, as well as the chip channel.

### C. 900-GHz Membrane Chip

A simplified Schottky model based on [48] is utilized for the design. An accurate 3-D model of the diode is drawn in HFSS, as shown in Fig. 6, and included in the simulation to model parasitics. The anode size on the measured chip is approximately  $0.4 \mu\text{m} \times 1.4 \mu\text{m}$ . The junction capacitance and parasitic capacitance,  $C_j$  and  $C_p$ , are approximately 1.5 and 0.25 fF, respectively. The measured series resistance,  $R_s$ , is  $35 \Omega$  at dc, as shown in Table II. The on-chip microstrip matching network in Fig. 7, consisting of high-impedance lines and a low-impedance line between the input  $E$ -plane probe and the diodes, provides the impedance matching of the diodes. The optimized low-impedance line is  $40 \Omega$  and high-impedance line is  $130 \Omega$ , respectively. The input return loss using on-chip matching network only without the optimized input waveguide is shown in Fig. 4 (dashed line without symbol) and the on-chip matching network is optimized around the center of the fundamental frequency. The input coupling is also carefully balanced between the two anodes to avoid overheating of any one anode in Fig. 8. The simulation shows that the generated fourth harmonic at the output is 20 dB less than the third harmonic when the fundamental is at 300 GHz.

### D. Micromachined Submillimeter-Wave Antenna

A corrugated or a diagonal horn would be ideal for the output interface, but they would require a complicated DRIE process or laser processing of the silicon substrate [29], [49]. We thus chose a rectangular horn consistent with the process steps of the tripler circuit. The horn allows for a quasi-optical interface that does not require waveguide mating at 900 GHz to measure the power. In the present setup (see Section IV), the horn is being used as a transition rather than a radiating antenna. The horn consists of a machined slope on the fixture and micromachined silicon blocks, including the output waveguide, transition, and aperture. Fig. 9(a) shows half of the horn split along the  $E$ -plane center. Fig. 9(b) depicts the silicon block on top of the fixture. Fig. 9(c) shows the silicon block only. In Fig. 9,  $\theta$  denotes the flare angle,  $t$  denotes the thickness of the silicon,  $a$  and  $b$  denote the opening of the aperture, and  $d$  denotes the length. The output waveguide

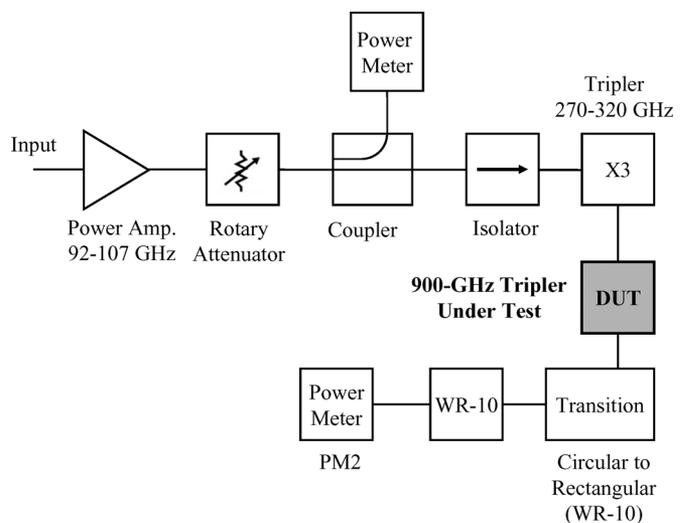


Fig. 14. Measurement consists of a  $W$ -band power amplifier, a rotary vane attenuator, a  $W$ -band coupler, an isolator, a WR-10 waveguide, a JPL in-house 300-GHz tripler, the 900-GHz tripler under test, a circular to rectangular waveguide (WR-10) transition, a WR-10 waveguide, and a PM2 power meter.

has the cross section of  $110 \mu\text{m} \times 230 \mu\text{m}$ . A full-wave simulation was performed using Ansoft HFSS. Table III shows the optimized parameters of the horn. The simulated far-field patterns of the horn (see Fig. 10) give  $H$ -plane peak copolarized sidelobes 17 dB down from the pattern peak and  $E$ -plane peak copolarized sidelobes 10 dB down from the pattern peak. The 3-dB half-beamwidth is  $10^\circ$ .

## III. FABRICATION AND ASSEMBLY OF THE COMPACT WAVEGUIDE CIRCUITS

In the fabrication process, a silicon-dioxide mask layer was deposited on both sides of the wafer using a plasma-enhanced chemical vapor deposition process. A photoresist layer was spun and patterned on the silicon-dioxide layer. The exposed silicon-dioxide layer was etched away using a dry-etching technique. The silicon was then etched using the DRIE technique. Backside patterning and etching completed the fabrication of

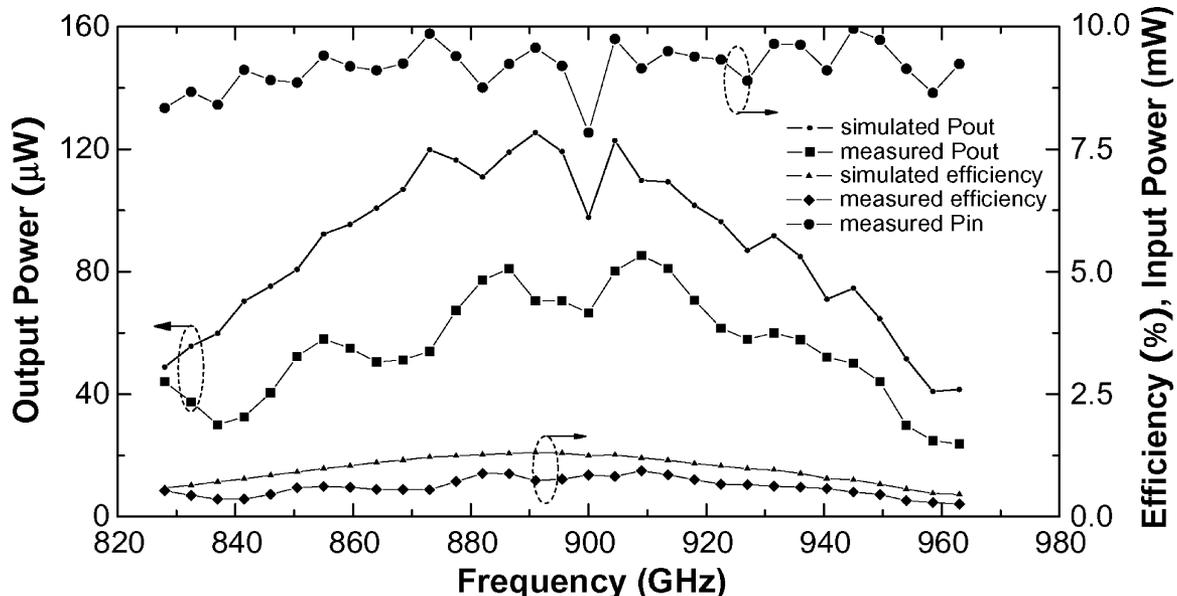


Fig. 15. Simulated and measured output power and efficiency at room temperature, as well as measured input power. No corrections have been made to the measured output power and efficiency numbers. At room temperature, the tripler is tested between 828–963 GHz and delivers more than 60  $\mu\text{W}$  between 877.5–922.5 GHz and the maximum output power of 85.3  $\mu\text{W}$ .

waveguide structure. A 3- $\mu\text{m}$ -thick metal layer of Ti/Cu/Au was sputtered on all surfaces of the micromachined block.

The chip's metallic beamleads are tack bonded to the silicon, and an image of the block and chip is shown in Fig. 11. The micromachined block is mounted on a fixture in Fig. 12 and aligned with two alignment pins. The fixture's input face adapts to a UG-387 waveguide flange. The output of the fixture is the aperture of the horn antenna. The tolerance of the input flange can lead to poor return loss [50], and an improved scheme for connecting the input waveguide to the silicon micromachined circuits, as suggested in [51], should further improve multiplier performance. SEM images of the silicon circuits are shown in Fig. 13.

#### IV. MEASUREMENT AND ANALYSIS

##### A. Measurement Setup

The measurement setup used for characterizing the 900-GHz tripler is shown in Fig. 14. A commercial synthesizer source in the  $W$ -band is amplified via a power amplifier and drives a broadband 300-GHz tripler [52]. An attenuator, coupler, and isolator are used to provide a constant 80-mW input signal to the 300-GHz tripler. This tripler generates 8–11 mW from 276 to 321 GHz.

A PM2 Erickson Instruments power meter [53] is used to measure the output power. The horn aperture is mated with a circular to rectangular waveguide. The diameter of the circular aperture is 0.093 in, and the length of the waveguide is 1.123 in, while the rectangular aperture is WR-10. An additional 1-in WR-10 waveguide connects this transition to the PM2.

##### B. 900-GHz Multiplier Performance

The input power to the 900-GHz tripler and the measured output power and efficiency are shown in Fig. 15. Simulated

values for efficiency and power are also shown. The simulated power only includes a 1.35-dB loss due to an imperfect fabrication process (surface roughness and deformation from the fabrication), as will be discussed in Section IV-C. Note that the measured power values have *not* been corrected for any losses due to the external waveguide transitions. The bias voltage of the 300-GHz tripler was optimized at each frequency to obtain maximum power. Conversion efficiencies were calculated by dividing the power levels recorded at the output of the 900-GHz chain by the power levels previously recorded at the output of the driver stage. The difference between the simulated and measured output power comes from the additional loss of the circular to rectangular waveguide transition 1-in waveguide mismatching at the input and output. The estimated losses in the external transitions are about 1.5 dB.

Different from the frequency response in Fig. 15, a measurement of the input power versus output power for the 900-GHz tripler is shown in Fig. 16, and the maximum observed output power is 109.3  $\mu\text{W}$  at 909 GHz. Again, no waveguide transition losses have been included.

##### C. Tolerance Analysis

At 900 GHz the wavelength is 300  $\mu\text{m}$ , and thus, precise control of the fabricated parts is very important. Fig. 13 shows the SEM images of the fabricated silicon waveguide structures. The surface roughness inside the waveguides is estimated to be about 1- $\mu\text{m}$  root mean square (rms).

The design of the tripler waveguide circuit takes account of dimensional variation between the ideal case and the fabricated structure. For example, the taper profile of the mask layers usually leads to an enlarged opening due to the limited selectivity of photoresist. This is accommodated by making the mask features appropriately smaller than the design values. Secondly, tolerances of the vertical striation and the reentrant angle in the DRIE

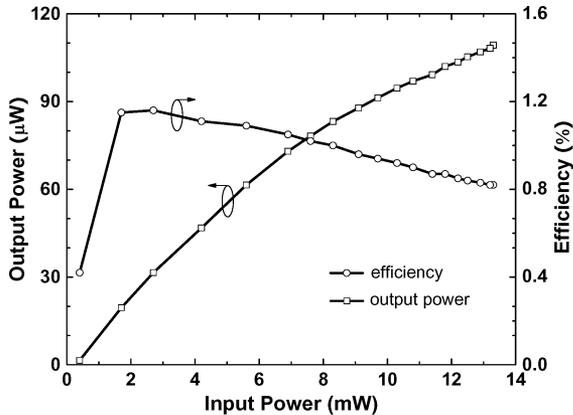


Fig. 16. Measured output power and measured efficiency versus input power at 909 GHz. The maximum observed output power is 109.3  $\mu\text{W}$ .

process can be reduced by optimizing the etching chamber pressure, the flow rate of gases, the time for etching and passivation, the power of etching and passivation, and the exposed area of silicon. Our process has been optimized to provide near-90° sidewalls.

The vertical striation worsens the surface roughness on the sidewall, which increases loss due to the skin effect. The surface roughness increases the total current path and leads to an increase in conductor loss, which is usually computed by [54]

$$\frac{\alpha_c}{\alpha_{c0}} = 1 + \frac{2}{\pi} \tan^{-1} \left( 1.4 \left( \frac{\Delta}{\delta} \right)^2 \right) \quad (1)$$

where  $\Delta/\delta$  is the normalized rms roughness. The conductor loss  $\alpha_{c0}$  can be estimated using a full-wave simulator. The skin depth of gold is about 120 nm at 300 GHz, and the estimated rms roughness on the sidewall is more than 1  $\mu\text{m}$ , as shown in Fig. 13(d). The total increased conductor loss is about 0.7 dB for the tripler.

Different from the vertical striation, the reentrant angle due to the lack of passivation on the sidewall leads to the deformation of the cross section and an impedance mismatch. However, our recipe results in near perfect 90° walls so the loss is substantially reduced. Besides the vertical striation and reentrant angle, the bottom of a dry-etched waveguide is not perfectly flat, as shown in Fig. 13(c). This leads to a very thin silicon brim left on the waveguide edges when the silicon wafer is etched through. Simulations of this irregularity revealed an additional estimated loss of 0.65 dB.

## V. CONCLUSION

A 900-GHz tripler using silicon micromachined blocks has been demonstrated with state-of-the-art performance close to the design specifications. The tripler delivers more than 60  $\mu\text{W}$  between 877.5–922.5 GHz and a maximum output power of 85.3  $\mu\text{W}$  (at room temperature with 80-mW drive around 100 GHz). In power sweep measurement, the tripler provides the maximum power of 109.3  $\mu\text{W}$  at 909 GHz. The expected maximum output power of this work and those in [39] and [40] are not the same due to the different number of tripler chips and anodes per chip, dc biasing schemes, and measurement

temperature. Successful demonstration of this tripler opens up the possibilities of using this approach for building high-performance and low-cost multipixel heterodyne receiver arrays.

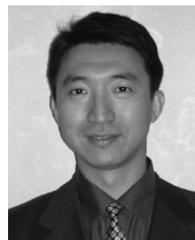
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