Design of a Wideband 6-Anode Frequency Tripler at 300 GHz with Optimum Balance

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Abstract

We report on the design methodology of a fix-tuned split-block waveguide balanced frequency tripler working nominally at 300 GHz. It features six GaAs Schottky planar diodes in a balanced configuration. The circuit will be fabricated with JPL membrane technology in order to minimize dielectric loading and insure an accurate and uniform thickness of the substrate. The multiplier power handling is limited by the breakdown voltage of the diodes that depends on the doping level of the active layer. With six diodes, the current choice for the doping level leads to medium power handling capabilities of about 50 mW. Increasing the number of diodes to eight would be an option but would lead to increased difficulties in design and fabrication. .

Introduction

This paper is linked to [1] that describes the design of a wideband fix-tuned 900 GHz waveguide frequency tripler optimized for medium-low input power (4 to 5 mW), and that is presented in the section "Astronomy, Atmospheric and Environmental Science" of this conference. It exposes the design methodology of a multi-diode balanced tripler at 300 GHz, to be used as the first stage of a 900 GHz local oscillator chain. By cascading two triplers, one can expect to reach almost 1 THz with enough power to drive SIS mixers, while keeping the number of stages to the minimum. If, in addition, the last stage is bias-less, then only a single bias supply is required for the multiplier chain. This is an advantage for implementing heterodyne receivers on large scale arrays like the Atacama Large Millimeter Array. Previous results have shown that such a cascade of balanced triplers is an interesting combination, especially above 1 THz [2], [3].

Multi diodes balanced design

The general design methodology can be found in [2], [3]. The block diagram of the 300 GHz tripler is given in Figure 1; with respect to the 900 GHz tripler described in [1], it features four additional diodes and an on-chip capacitor to decouple the DC bias voltage to the high frequency signals. This section will focus on the specificities of designing balanced triplers with more than two diodes.

In our tripler designs, the diodes are in series at DC but, due to the symmetry of the circuit, they appear to be in an anti-parallel configuration at RF frequencies. This topology is equivalent to the one proposed in [4], but has the advantage to easily allow more than two diodes to be implanted on chip. More diodes mean increased power handling capabilities. A first example of a working 4-diode frequency tripler at 600 GHz can be found in [5]. There are limits anyway: the number of diodes is constrained by the width of the chip-channel and the diode's physical dimensions. The width of the channel is one of the parameters that define the cutoff frequencies of parasitic modes.

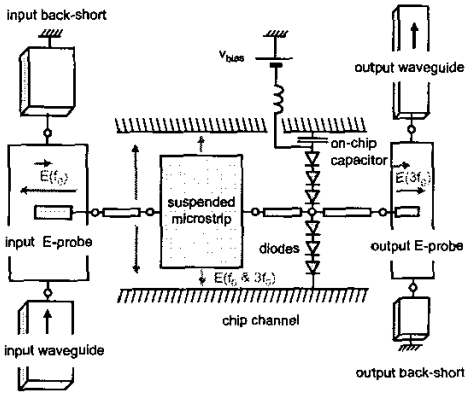

Fig. 1: Block diagram of the 300 GHz balanced tripler. Inside the chip channel, only a quasi-TEM mode should propagate at all the frequencies of interest.

Each diode needs to be properly matched at all the relevant frequencies, i.e. the fundamental and its first two harmonics; the matching at the second harmonic is of prime importance [6] and can only be achieved by optimizing the distance between the diodes and the channel cross-section dimensions. The width of the air-bridges used to connect the anodes is also a parameter of optimization. In addition, the input power needs to be evenly shared between the diodes to guaranty that no diode is overdriven.

Optimization method

The first step is to optimize the diodes cell that consists in the part of the circuit that includes the diodes, a section of the chip-channel and two sections of the propagating line at the center of the chip (see Figure 2). The optimization is performed using 3D

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electromagnetic codes like Ansoft HFSS 9.1 and harmonic-balance codes like Agilent ADS. The optimum diode junction capacitance and bias voltage is also determined at the same time. This optimization is performed for a given input power and output frequency. In this particular case, due to the initial choice of a medium doping level (3E17 cm^{-3}) for the wafer (that will feature higher frequency multipliers), only 50 mW of input power could be safely handled by six diodes (expected break-down voltage is -7V per diode).

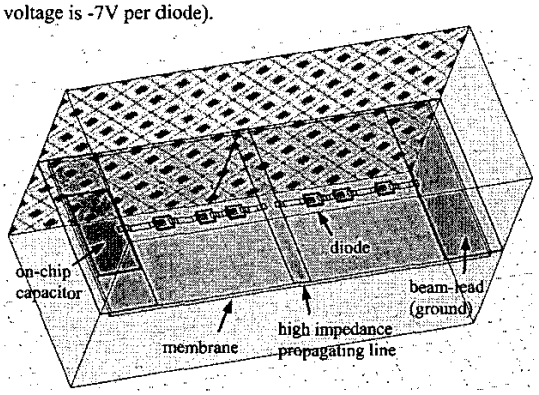

Fig. 2: Diode's cell used to optimize the channel cross-section dimensions, the location of the 6 anodes and the air-bridge size. One of the HFSS ports is shown in the back side of the diode's cell.

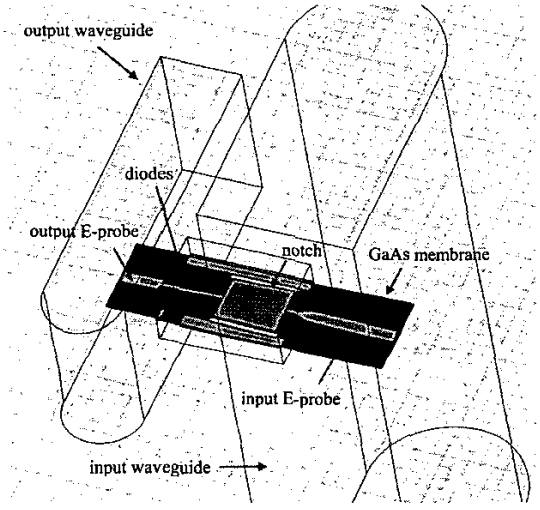

Fig. 3: 3D view of the 300 GHz tripler as modeled with HFSS. The chip is held by two beam leads. The chip dimensions are 0.33×1.1 mm.

The optimization is semi-empirical since no equivalent model of the diode's cell has been built. It necessitates many 3D electromagnetic simulations that are greatly facilitated by the possibility to parameterize the full 3D structure with HFSS 9.1. For this topology a basic rule was found: the optimum Cj0 per diode is linked to the channel cross-section perimeter; the longer the perimeter the smaller the junction capacitance. It is noticeable that the height of the channel is a parameter that has a great influence on the matching of the diodes but much less on the cutoff frequency of the parasitic modes inside the chip-channel. It can therefore be easily adjusted to optimize the performances.
The other rule is that the diodes should be separated by slightly uneven distance (due to the physical size of the mesas that breaks partially the symmetry) as shown in Figure 2.

The second step is to optimize the input and output matching circuit using on-chip and waveguide matching elements. Details about the method are given in [2] and [3].

At the current stage of the optimization, the expected peak efficiency is almost 20% but the bandwidth is narrow, of about 5%. Work has to be done to better optimize the input coupling. Based on previous results at 600 GHz [5], about 15% of bandwidth should be feasible. A good balance between the diodes at the input and the output frequencies has been successfully achieved. A 3D view of the current version of the multiplier is shown in Figure 3.

Conclusion

The design of a six-diode tripler at 300 GHz with an expected efficiency of 20% has been documented. This topology could be used at lower frequencies with an increased number of diodes to handle more power.

This work has been carried out at LISIF, Université Paris VI, in collaboration with Jet Propulsion Laboratory, California Institute of Technology.

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