

A High-Power Wideband Cryogenic 200 GHz Schottky “Substrateless” Multiplier: Modeling, Design and Results

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Abstract — A high-power doubler for the frequency band 184 to 212 GHz has been fabricated and tested. Circuit measurements give an output power over 30 mW across the band with peaks above 50 mW at 100 K. Even better results are expected from future testing under cryogenic conditions at approximately 100 K ambient. The multiplier is a high power design used as a first stage for multiplier chains spanning the frequency range of 1 to 3 THz. It is based on the “substrateless” monolithic integrated circuit topology developed at JPL. Its strength is passive circuitry with lower-loss than conventional MMICs, due to the removal of the semiconductor substrate from beneath most of the metallic traces. Further, it facilitates the optimum design of broadband multipliers by simplifying the transitions between waveguide and diode sections of the circuit. Since the multipliers are operated at relatively high input power (up to 250 mW), low temperature (down to 100 K) and wide bandwidth (14 %), accurate analysis of the doubler characteristics affected by these conditions is important. The results of the continuing JPL Schottky diode physical modeling effort are discussed, including the effects of temperature and high power operation. A thermal analysis of the doubler is also shown.

I. INTRODUCTION

Currently there is a demand for wide-bandwidth frequency multiplier chains [1-3] with outputs above 1 Terahertz for use in sub-millimeter wave heterodyne receivers. These space-borne radiometers are primarily intended for astrophysical observation. The Jet Propulsion Laboratory maintains a continuous effort to develop and implement novel technologies to produce robust, reliable and repeatable planar Schottky diode multipliers for these applications [4]. In order to produce useable power at the ultimate output frequency, the first stage in the chains are being pumped with powers of 200 mW and above at W-band [5]. This paper will focus on a few of the consequences and requirements of operating at these high power levels. Specifically, high-power multipliers must operate at temperatures far from room temperature. For multiplier blocks at room temperature, the Schottky junction temperatures which determine their behavior will be much higher. It is desirable to operate the multiplier substantially below room temperature, both to improve the performance and to reduce thermal stress on the semiconductor devices. The issue of optimization of diode characteristics at various temperatures will be addressed.

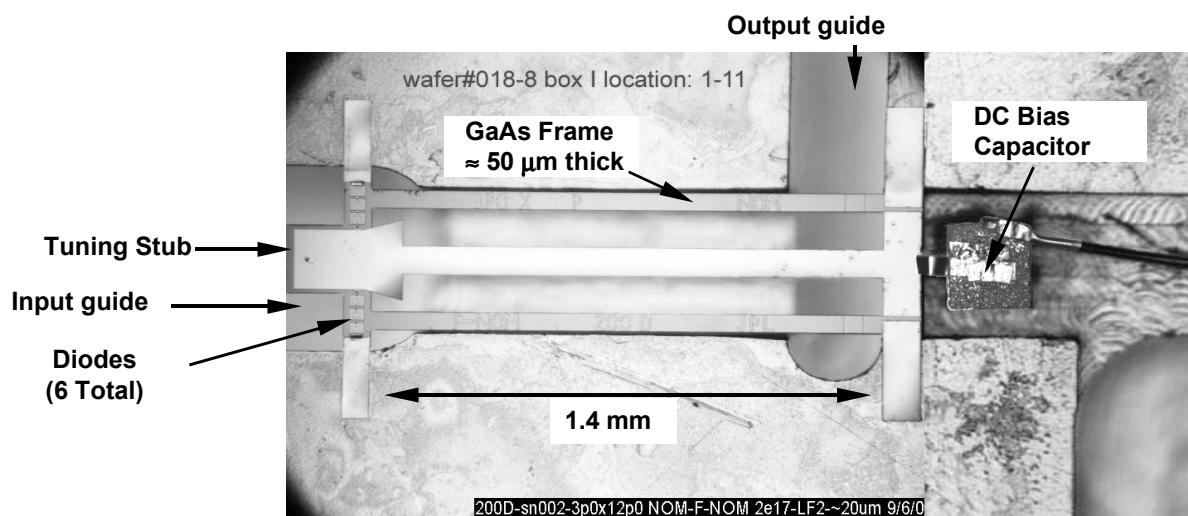


Figure 1. Photo of 200 GHz substrateless doubler in split waveguide block.

II. DESIGN AND PERFORMANCE

The multiplier consists of two components – the nonlinear solid state devices (Schottky diodes), analyzed using harmonic balance simulators, and the surrounding passive input, output and impedance matching circuitry, which is analyzed using the HFSS finite element electromagnetic simulator. The circuit design process has been discussed previously [5–7] as has been the fabrication [8]. Figure 1 shows the 200 GHz doubler mounted in the bottom half of the split block. In order to allow matching and to distribute the power, the circuit employs six diode anodes in a linear array. The diodes are integrated with metallic circuitry using a GaAs MMIC process. Additional passive matching is accomplished in waveguide. The lines fabricated on GaAs act as waveguide transitions as well as part of the impedance matching, and much of it is etched away in the “substrateless” process as discussed in the earlier references.

The doubler uses a balanced planar diode configuration [9,10], incorporating symmetrical series of diodes configured so that they only respond to odd harmonics at the input and even harmonics at the output. This greatly enhances separation of the input and output signal frequencies. This not only simplifies the circuits, but enables wide band design, since almost no additional frequency filtering is forced to be included in the impedance matching circuitry.

III. THERMAL MODEL

The doubler was designed for an input power of 200 mW, and the test input power was greater than 200 mW over part of the band. In order to analyze the multiplier, the actual junction operating temperatures must be known. Additionally, the junction temperature must be determined to verify that the power level and diode temperature will not destroy the devices with operation over long periods of time. To estimate the anode temperature, a basic one-dimensional “series-resistor” model has been developed. It is essentially a finite-difference model solved iteratively. The system analyzed is depicted schematically in Figure 2a. Since the chip is symmetrical about the center plane in the input waveguide, only half has been analyzed, with no heat assumed to flow across the symmetry plane. Knowing the input power and circuit efficiency gives the dissipated power and combining this with the block temperature gives the temperatures of the devices.

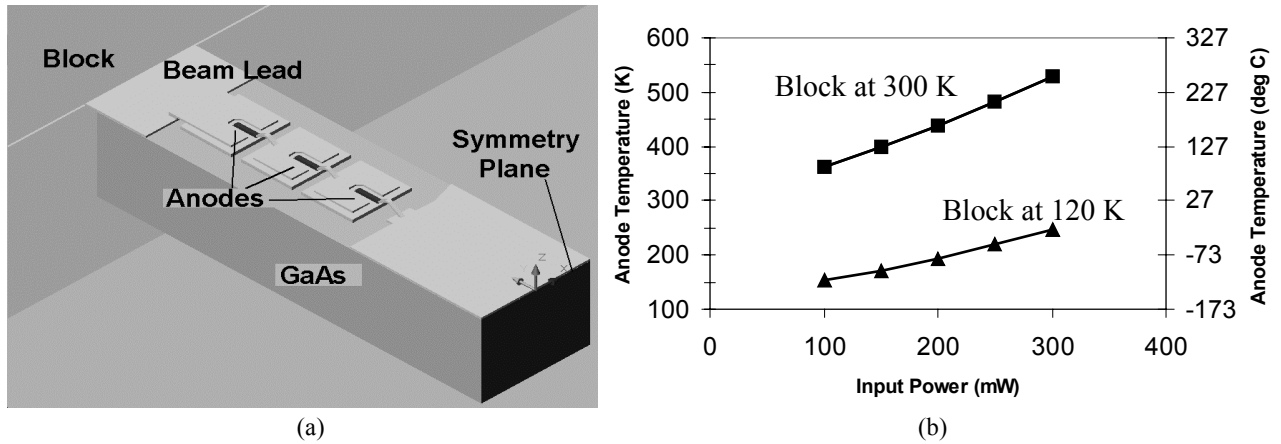


Figure 2. 200 GHz doubler thermal model. (a) Schematic. The anodes are heat sources and the block is a heat sink. No heat flows across all other surfaces. (b) Calculated worst case anode temperature. Block at 120 and 300 K.

Further assumptions are that all anodes dissipate the same power, and that radiation and convection can be neglected. Published thermal conductivity data for undoped GaAs between 100 to 600 K has been used, and the effect of doping neglected since almost all of the frame is semi-insulating material. The thermal conductivity of GaAs decreases with temperature in this temperature range. It is assumed that the beam lead is a 1.5 μm thick and 70 μm wide ribbon of gold, and that a gap of 8 μm separates the frame from the block wall.

Shown in Figure 2b are maximum anode temperature as a function of input power, based on an assumed 25 percent conversion efficiency. Traces for ambient temperatures of 120 and 300 K are shown. This indicates that operation at room temperature is marginal, but at 120 K the multiplier should run quite cool.

IV. DIODE MODEL INCLUDING CURRENT SATURATION

For the Herschel Space Observatory it has been decided to operate at a low temperature, both for thermal margin and to get improved multiplier performance [11]. We have a continuing effort at JPL to improve the modeling of the diodes, specifically including temperature and high frequency effects. Most of the elements of the model have been covered earlier [12–14], but the time dependence of current saturation in the undepleted epitaxial region has not been previously included in our multiplier design. A basic model has been developed for this purpose.

Current saturation at high fields in GaAs results from the *decrease* in velocity with field once a threshold field around 5 kV/cm has been reached. This is due to electrons gaining enough energy from the field to scatter into the upper low-mobility valleys of the electron conduction band. This acts as a current limit in the undepleted epitaxial region of the diode. Current saturation reduces the efficiency of the diode as a multiplier by impeding the ability of the charge at the edge of the depletion region to move with the pump signal, resulting in a decrease of the varactor capacitance non-linearity.

Usually current saturation, including transient effects, are modeled using the Monte Carlo method [15, 16]. Since Monte Carlo calculations take large amounts of computer time, it is desirable to incorporate these effects into a harmonic balance (HB) circuit simulator using a simple model which can be rapidly integrated using the Runge-Kutta type integrators normally used in HB simulators. To do this, we start first with the steady-state field dependent velocity. There are several equations describing velocity saturation; the simplest and oldest is the Kramer and Mircea formula [17]:

$$v(E) = \frac{\mu_0 E + v_s (E/E_N)^4}{1 + (E/E_N)^4} \quad (1)$$

where v is the velocity, E the magnitude of the electric field, v_s the ultimate saturation velocity at about 20 kV/cm, and E_N is a characteristic field which determines where the peak velocity occurs. In order to use this equation, the parameters of equation (1) are determined from single particle Monte Carlo simulations for each combination of dopant concentration and temperature [18]. To model the velocity behavior of the electrons over a pump cycle we use a time constant based formulation somewhat similar to that introduced in [19]. The epi current is divided between two resistances representing the dominant two conduction band valleys in which electrons travel, as illustrated in Figure 3.

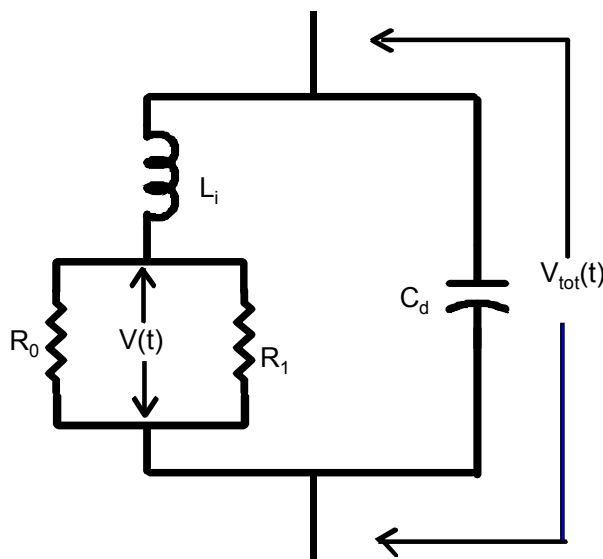


Figure 3. Model of undepleted epi. R_0 and R_1 are proportional to $1/\mu_0$ and $1/\mu_1$.

Defining μ_0 as the lower valley mobility, (about 4000 cm²/Vs or higher at reduced temperatures), and μ_1 is the upper valley mobility (about 200 cm²/Vs) and n_0 and n_1 as the corresponding valley electron populations, the velocity in equation (1) can be written:

$$v(E,t) = \left[\mu_0 \frac{n_0(E,t)}{n} + \mu_1 \frac{n_1(E,t)}{n} \right] E(t) \quad (2)$$

with n the total electron concentration in the undepleted epi. Then, several coupled differential equations are used to represent the time-dependent behavior of the velocity. The upper valley population is described by:

$$\frac{dn_1}{dt} = \frac{n_{1s}(E) - n_1(t)}{\tau} \quad (3)$$

where $n_{1s}(E)$ represents the static population of the upper valley, derived by combining equations (1) and (2) (without time-dependence) and considering that the total electron concentration is the sum of the populations of the two valleys: $n = n_0 + n_1$. $E(t)$ is the instantaneous voltage seen by the electrons (inside the carrier inertia inductance), and is found from V by dividing it by the undepleted epi-layer thickness, t_{UD} , also time-dependent. The time constant, τ , depends on E and on $n_{1s}(E) - n_1(t)$; a simple formula for τ is fit to a time-dependent ensemble Monte Carlo calculation [16].

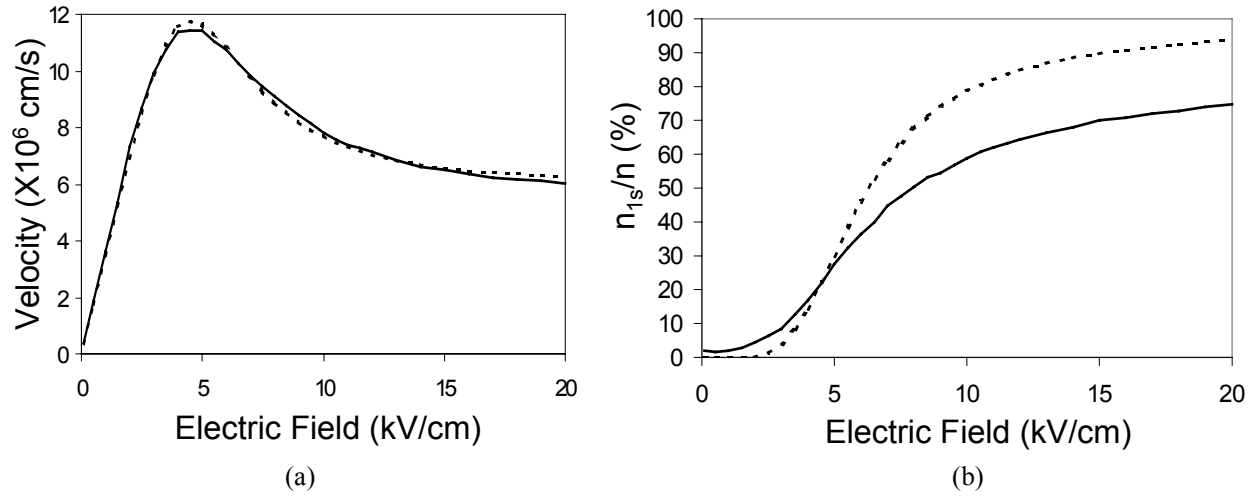


Figure 4. Static simulation parameters for $N_D = 1 \times 10^{17}$ at 439 K. Solid lines are Monte Carlo calculations, broken lines are fitted as described in the text. (a) Velocity, (b) Upper valley population fraction.

A typical plot of the static velocity, $v(E)$, from the Monte Carlo simulation and a fitted version of equation (1) for $N_D = 1 \times 10^{17}$ cm⁻³ and $T = 439$ K is shown in Figure 4. Also shown are the Monte Carlo and calculated versions of $n_{1s}(E)$. The difference between the Monte Carlo and formula version for n_{1s} is explained by considering the total electron population. Once a substantial fraction of electrons inhabits the upper valley, a smaller fraction decays back into the lower valley, a state of dynamic equilibrium. These “decayed” electrons have a large energy and velocity spread, but their *average* velocity is characteristic of the upper valley, i.e. it is low due to the low upper valley mobility. Since the purpose of the calculation is to use the total aggregate velocity to find the current, the higher “effective” upper valley population fraction from the formula is paired with the low mobility in equation (2), and the smaller “effective” lower valley population is assumed to have a high velocity consistent with the lower valley mobility.

The current through the inductor representing carrier inertia depends on the total epi voltage, V_{tot} :

$$\frac{di}{dt} = \frac{V_{tot}(t) - V(t)}{L_i} \quad (4)$$

where L_i is the carrier inertia inductance, equal to:

$$L_i = \frac{m^* t_{UD}}{q^2 n A} \quad (5)$$

with m^* the effective mass and A the area of the diode. The total current through the inductance is:

$$i = qnvA. \quad (6)$$

To simulate the full diode two other differential equations must be included to model the undepleted epi capacitance, as well as the junction capacitance [12], for a total of four differential equations. Additionally, the influence of current tunneling through the Schottky barrier is included in the junction conduction current [14, 20]. In the forward direction, it is calculated using the ideality factor and reverse saturation current in the usual thermionic emission equation [21]. However, a barrier height reduction is included to model the average electron emission energy being slightly below the actual barrier peak due to quantum mechanical tunneling [20]. In the reverse direction the calculations described in [14] are fitted to a simple power law voltage-dependent effective barrier height for each combination of doping concentration and temperature. The resultant equation is:

$$J = J_s \left\{ \exp\left(\frac{qV}{\eta kT}\right) - \exp\left[-\text{sign}(V) \left|\frac{V}{V_{tr}}\right|^m\right] \right\} \quad (7)$$

with the saturation current given by:

$$J_s = A^* T^2 \exp\left[-\frac{q(\phi_{be0} + \Delta\phi_{be0})}{kT}\right] \quad (8)$$

The ideality factor, η , and the barrier offset at $V=0$, $\Delta\phi_{be0}$, are determined from forward current calculations, and V_{tr} and m from the reverse current. Typical values are, for $N_D = 1 \times 10^{17} \text{ cm}^{-3}$ and $T = 439 \text{ K}$: $\eta = 1.13$, $\Delta\phi_{be0} = -0.026 \text{ eV}$, $V_{tr} = 0.624 \text{ V}$, $m = 0.774$. The other parameters are the effective Richardson constant, $A^* = 7.8 \text{ A/cm}^2/\text{K}^2$, and the effective zero-bias barrier height, ϕ_{be0} , which is derived from previous measurements [14].

The temperature-dependent breakdown voltage calculations described in [14, 22] were also fitted to a simple formula, valid only for GaAs from 100 to 500 K:

$$V_{BR} = (33.166 + 0.05224T) \left(\frac{N_D}{10^{16} \text{ cm}^{-3}}\right)^{-0.76} + 6.126 - 0.00333T \quad (9)$$

Currently, it appears that the above model is difficult to incorporate into commercial harmonic balance (HB) simulators. Therefore a version of the Siegel/Kerr reflection algorithm HB simulator [23] has been written, and the model incorporated into it. Figure 5 shows an example of a waveform result for a 200 GHz doubler. The anode size is $3 \times 12 \mu\text{m}^2$, doping is $1 \times 10^{17} \text{ cm}^{-3}$ and the temperature of the block is 300 K, resulting in a junction temperature of 439 K according to the thermal model. The voltage and current waveforms are depicted in Figure 5a, and Figure 5b shows the

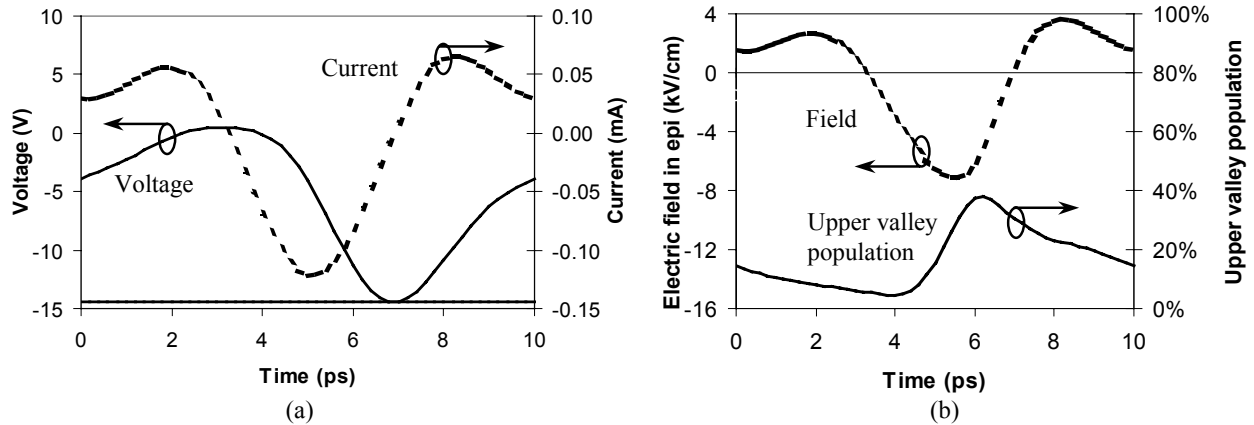


Figure 5. Variation of diode parameters during pump cycle: (a) junction voltage and current. (b) undepleted epi electric field and upper valley population fraction.

variation of electric field in the undepleted epitaxial region during one cycle, as well as the upper valley electron population fraction. Two critical points must be made. First, for this relatively small anode, the voltage waveform

minimum is the breakdown voltage, plotted as the straight line across the graph at -14.4 volts. The optimizer is configured so that the minimum voltage will not fall below the breakdown, which is accomplished by adjusting the bias, while optimizing the embedding impedances for maximum efficiency. Also note that the electric field magnitude exceeds 7 kV/cm. Comparing to the velocity/field plot in Figure 5, it is clear that some current saturation must occur, which can be observed in the upper valley population fraction which reaches about 40 percent. As the temperature is lowered this ceases to be a factor for this diode since a lower potential is developed across the undepleted epi, due to the increase in both mobility and maximum velocity at low temperature.

The first use for this HB program is to determine what doping concentration would be optimum for a given temperature and frequency range. Analyzing several diode sizes at 1×10^{17} and 2×10^{17} cm^{-3} doping at block temperatures of 120 and 300 K (corresponding to 194 and 439 K junction temperatures) results in the plots in Figure 6. Optimized efficiency is

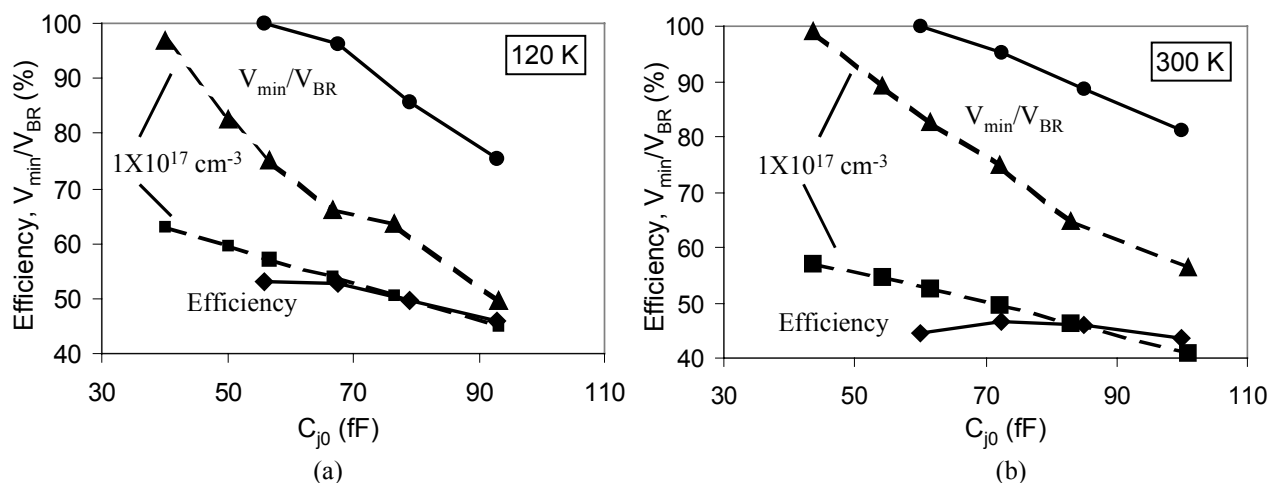


Figure 6. Optimized 200 GHz doubler efficiency and ratio of minimum voltage to breakdown voltage for $N_D=2 \times 10^{17}$ (solid lines) and $N_D=1 \times 10^{17}$ (broken lines) cm^{-3} for block temperatures of (a) 120 K and (b) 300 K.

plotted against zero-bias junction capacitance, which gives a measure of the circuit impedance. The input power is fixed at 33 mW per anode at 100 GHz. Since the minimum voltage must be limited to the breakdown voltage, the $2 \times 10^{17} \text{ cm}^{-3}$ diode saturates as the diode is made smaller, even at lower temperature. On the contrary, for the $1 \times 10^{17} \text{ cm}^{-3}$ diode, the minimum voltage limit is not reached until a substantially higher efficiency is achieved. While it is possible that a lower doping still would give even better efficiency, the current saturation would give diminishing returns, at least at room temperature. Also, it should be noted that none of this analysis addresses the ease or difficulty of creating a broadband design for these diode impedances. This question requires going through the design process to answer. If we take the input Q as an indicator, with lower Q corresponding to wider achievable bandwidth, for these two dopings and temperatures the Q is roughly independent of doping, temperature, and diode size at about 7 to 8. The exception is that the small, saturated $2 \times 10^{17} \text{ cm}^{-3}$ diodes have lower Qs, dropping to around 5.

IV. RESULTS

The measured performance of one 200 GHz doubler is shown in Figure 7. It was fabricated using $3 \times 12 \mu\text{m}^2$ diodes on $2 \times 10^{17} \text{ cm}^{-3}$ doped material, resulting in a room temperature C_{j0} of 60 fF. The measurements were made at block temperatures of 120 and 300 K. The peak power at 120 K is around 50 mW, and the efficiency is around 30 percent over a broad band. It will be noted that at some frequencies there is almost no improvement in performance at low temperature, whereas at others there is a substantial improvement.

Also included is the calculated efficiency based on this diode modeling, and including the HFSS models of the passive circuitry. One limitation of the current software is that only one diode can be included, so the diodes must be combined in some way. Advantage is taken of the symmetry of the balanced circuit, so the HFSS S-parameter blocks have only three

diode ports. These are tied together and impedance transformed to be with a single diode in the same technique that is used in the initial linear circuit design [24]. Despite this limitation, the calculated results approximate the measurements fairly well, including the temperature dependence. The efficiency variation with temperature decreases gradually with increasing frequency. This is most likely due to the decreasing magnitude of the parasitic conduction current (forward and reverse) as the input power decreases with frequency. This is also observed in the decreasing bias current at lower

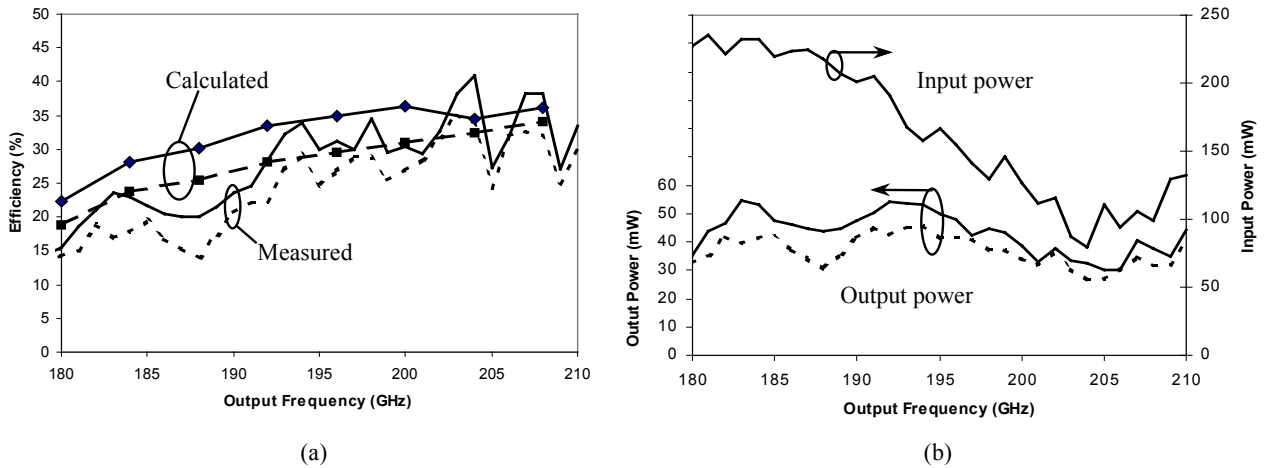


Figure 7. Performance of 200 GHz doubler, anode $3 \times 12 \mu\text{m}^2$, $N_D=2 \times 10^{17} \text{ cm}^{-3}$, 120 K(solid lines), 300 K(broken lines). (a) Calculated and measured efficiency. (b) Input and output powers.

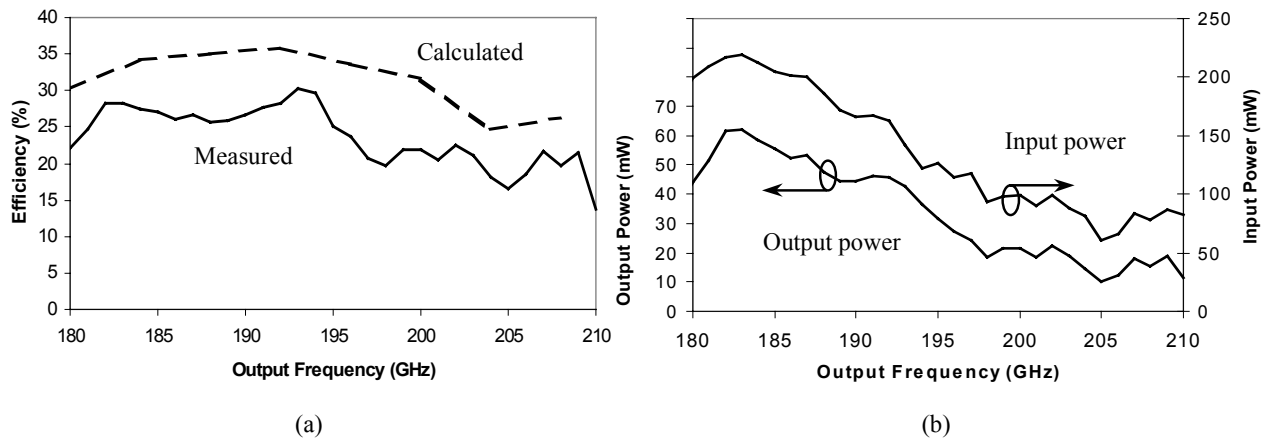


Figure 8. Performance of 200 GHz doubler, anode $3 \times 14.4 \mu\text{m}^2$, $N_D=2 \times 10^{17} \text{ cm}^{-3}$, 300 K. (a) Calculated and measured efficiency. (b) Input and output powers.

input powers. With no conduction current, the primary limit on efficiency is the series resistance, which is only weakly temperature-dependent. This was noted in reference [14] where a similar size diode was found to have a series resistance essentially independent of temperature.

A second doubler incorporating $3 \times 14.4 \mu\text{m}^2$ diodes also on $2 \times 10^{17} \text{ cm}^{-3}$ material was measured at room temperature only, with results shown in Figure 8. Again, the simulation gives a good approximation of its performance, which yielded over 60 mW peak output power.

V. CONCLUSION

Measured results of the performance of wide-band high-power 200 GHz doublers have been presented with peak power of 50 mW and peak efficiency over 30 percent. A thermal analysis indicates the doubler will not over heat, especially if cooled to 120 K. A temperature-dependent diode model useful for high power and frequency has been described and tested.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the technical assistance of Dr. Neal Erickson, the assembly work of Ray Tsang and the testing assistance provided by William Chun.

The research described in this publication was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

REFERENCES

- [1] E. F. van Dishoek and F. P. Helmich, "Scientific drivers for future high-resolution far-infrared spectroscopy in space," *Proc. 30th ESLAB Symp., Submillimetre and Far-Infrared Space Instrumentation 1996*, ed. E. J. Rolfe, ESA SP-388, pp. 3-12.
- [2] G. Pilbratt, "The FIRST mission," *Proc. ESA Symp., The Far Infrared and Submillimetre Universe 1997*, ESA SP-401.
- [3] N. D. Whyborn, "The HIFI Heterodyne Instrument for FIRST: Capabilities and Performance," *Proc. ESA Symp, The Far Infrared and Submillimetre Universe 1997*, ESA SP-401.
- [4] I. Mehdi, E. Schlecht, A. Arzumanyan, J. Bruston, P. Siegel, R. Peter Smith, J. Pearson, S. Martin and D. Porterfield, "Development of millimeter and submillimeter-wave local oscillator circuits for a space telescope," *Proc. SPIE*, vol. 3795, pp. 329-337, *Terahertz and Gigahertz Photonics*, R.J. Hwu, K. Wu, Eds., October 1999.
- [5] E. Schlecht, G. Chattopadhyay, A. Maestrini, A. Fung, S. Martin, D. Pukala, J. Bruston and I. Mehdi, "200, 400 and 800 GHz Schottky Diode "Substrateless" Multipliers: Design and Results," *IEEE Int. Microwave Symp. Digest*, pp. 1649-1652, Phoenix, AZ, May 2001.
- [6] J. Bruston, R.P. Smith, S.C. Martin, A. Pease and P.H. Siegel, "Progress Toward the Realization of MMIC Technology at Submillimeter Wavelengths: A Frequency Multiplier to 320 GHz," *Proc. IEEE Intl. Microwave Symp. Digest*, Baltimore, MD, June 1998, pp. 399-402.
- [7] D. Porterfield, T. Crowe, R. Bradley, N. Erickson, "An 80/160 GHz Broadband, Fixed-Tuned Balanced Frequency Doubler," *IEEE Int. Microwave Symp. Digest*, Baltimore, MD, June 1998, pp. 391-394.
- [8] S. Martin, B. Nakamura, A. Fung, P. Smith, J. Bruston, A. Maestrini, F. Maiwald, P. Siegel, E. Schlecht and I. Mehdi, "Fabrication of 200 to 2700 GHz Multiplier Devices Using GaAs and Metal Membranes," *2001 Int. Microwave Symp. Digest*, pp. 1641-1644, Phoenix, AZ, May 2001.
- [9] B.J. Rizzi, T.W. Crowe, and N.R. Erickson, "A High-Power Millimeter-Wave Frequency Doubler Using a Planar Diode Array," *IEEE Microwave Guided Wave Lett.*, vol.3, pp. 188-190, June 1993.
- [10] N.R. Erickson, "Diode Frequency Multipliers for Terahertz Local Oscillator Applications," *Proc. SPIE*, vol. 3357, pp. 75-84, *Advanced Technology MMW, Radio, and Terahertz Telescopes*, T.G. Phillips, Ed., July 1998.
- [11] A. Maestrini, D. Pukala, F. Maiwald, E. Schlecht, G. Chattopadhyay, and I. Mehdi, "Cryogenic operation of GaAs based multiplier chains to 400 GHz," *Eighth International Terahertz Conference*, Darmstadt, Germany, September 2000.
- [12] T.W. Crowe, "GaAs Schottky Barrier Mixer Diodes for the Frequency Range 1-10 THz," *Int. J. Infrared Millimeter Waves*, vol. 10, no. 7, pp 765-777 (1989)
- [13] J.T. Louhi and A.V. Räisänen, "On the Modeling and Optimization of Schottky Varactor Frequency Multipliers at Submillimeter Wavelengths," *IEEE Trans. Microwave Theory Tech.*, vol. 43, no. 4, pp 922-926, 1995.
- [14] E. Schlecht, F. Maiwald, G. Chattopadhyay, S. Martin and I. Mehdi, "Design Considerations for Heavily-Doped Cryogenic Schottky Diode Varactor Multipliers," *Twelfth International Symposium on Space Terahertz Technology*, San Diego, CA, February 2001.
- [15] T.J. Maloney and J. Frey, "Transient and Steady-State Electron Transport Properties of GaAs and InP," *J. Appl. Phys.*, vol. 48, p 781, 1975.
- [16] R.O. Grondin, P.A. Blakey, J.R. East, "Effects of Transient Carrier Transport in Millimeter-Wave GaAs Diodes," *IEEE. Trans. Electron Devices*, vol. ED-31, no. 1, pp 21-28, 1984.
- [17] B. Kramer and A. Mircea, "Determination of Saturated Electron Velocity in GaAs," *Appl. Phys. Lettr.*, vol. 26, no. 11, pp 623-625, 1975.
- [18] J. East and I. Mehdi, "Temperature Effects in Varactors and Multipliers," *Twelfth International Symposium on Space Terahertz*

Technology, San Deigo, California, February, 2001.

- [19] D.E. McCumber and A.G. Chynoweth, "Theory of Negative-Conductance Amplification and of Gunn Instabilities in "Two-Valley" Semiconductors," *IEEE Trans. Electron Dev.*, vol. ED-13, no. 1, pp 4-21, 1966.
- [20] U.V. Bhapkar and R.J. Mattauch, "Numerical Simulation of the Current-Voltage Characteristics of Heteroepitaxial Schottky Barrier Diodes," *IEEE Trans. Electron Devices*, vol. 40, no. 6, 1993.
- [21] S.M. Sze, *Physics of Semiconductor Devices*, 2nd Ed., Chapter 5, Wiley, New York, 1981.
- [22] G.E. Stillman, and C.M. Wolfe, "Avalanche Photodiodes," in *Semiconductors and Semimetals Volume 12*, ed. R.K. Willardson, and A.C. Beer, Academic Press, New York, 1977.
- [23] P.H. Siegel, A.R. Kerr, W. Hwang, "Topics in the Optimization of Millimeter-Wave Mixers," NASA Technical Report NASA-TP-2287, NAS 1.60:2287, March, 1984.
- [24] D.W. Porterfield, *Millimeter-Wave Planar Varactor Frequency Doublers*, p. 49, Ph. D. Dissertation, University of Virginia, 1998.