An 800 GHz Broadband Planar Schottky Balanced Doubler

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Abstract

A broadband planar Schottky balanced doubler at 800 GHz has been designed and built. The design utilizes two Schottky diodes in a balanced configuration on a 12 μm thick Gallium Arsenide (GaAs) substrate as supporting frame. To minimize dielectric loading of the waveguides and to reduce RF losses in passive circuit elements, a new fabrication technology is used where the GaAs substrate under the transmission lines is removed during the back-side processing, leaving free standing metal lines suspended in air from GaAs frame. Metal beamleads are used for DC and RF contacts with the waveguides, and they allow the doubler chip to be dropped inside the split waveguide block, making assembly procedure relatively simple, fast, and robust. This broadband doubler (designed for 735 GHz to 850 GHz) achieved more than 10% efficiency at 770 GHz, giving 1.1 mW of peak output power when pumped with about 9 mW of input power at room temperature. This represents the best performance from any doubler at these frequencies to date in literature.

I. Introduction

At millimeter and submillimeter wavelengths quite a few new instruments are being built for astronomical, remote sensing, atmospheric, and planetary missions. Generally, heterodyne detectors are the receiver of choice for these instruments, which use cryogenically cooled superconductor insulator superconductor (SIS) and and hot electron bolometer (HEB) mixers. All these heterodyne receivers require fixed-tuned broadband local oscillator (LO) sources which are robust, easy to implement, cryogenically coolable, and reliable. Reliability of the LO sources is a very important issue, specifically for the space missions.

Current state-of-the-art solid state sources above 200 GHz are constructed from chains of cascaded Schottky-barrier varactor diode frequency multipliers. Using a new planar *substrateless* technology [1], we have designed and developed an 800 GHz broadband doubler for use in the 735 GHz to 850 GHz frequency range. The motivation for designing a doubler in this frequency range is many fold. We want to use this doubler as a LO source to pump ground-based SIS receivers like Caltech's CSO and the ASTRO instrument at the south pole. Spectroscopic studies at these frequencies is very important from astronomical perspective, as there are quite a few rotational transition lines in the molecular clouds in the interstellar medium in this frequency range. They are the **CO 7 → 6** transition line at 807 GHz, the **C** transition line at 809 GHz, and the $\mathbf{CH^+}$ transition line at 835 GHz. We also want to use this doubler as a drive stage for a 1600 GHz doubler where the interest is at 1612 GHz for the **CO 15 → 14** rotational transition line. We also intend to use this doubler to drive a 2400 GHz tripler where the astronomical interest is for the $\mathbf{N^+}$ **2 → 1** transition line at 2460 GHz.

This 800 GHz balanced doubler incorporates two symmetrical pair of diodes configured in such a way that they only respond to odd harmonics at the input and even harmonics at the output, making it easier to separate the input and output frequencies without any filter structure [2]. The balanced design also makes the broadband design possible. The only disadvantage of a balanced configuration is that it requires a minimum of two diodes, requiring more input power to pump the doubler. Since at these frequencies high pump power is not easily available, there is a line of thought which advocates single diode design, pointing to the fact that a single diode could be pumped to sufficient no-linearity for optimum efficiency with low available input power. However, our experience in this frequency range has shown that the loss in the filter structure for the single diode design is too high and it negates other advantages of the single diode design. Hence, we decided to incorporate a balanced design for our doubler.

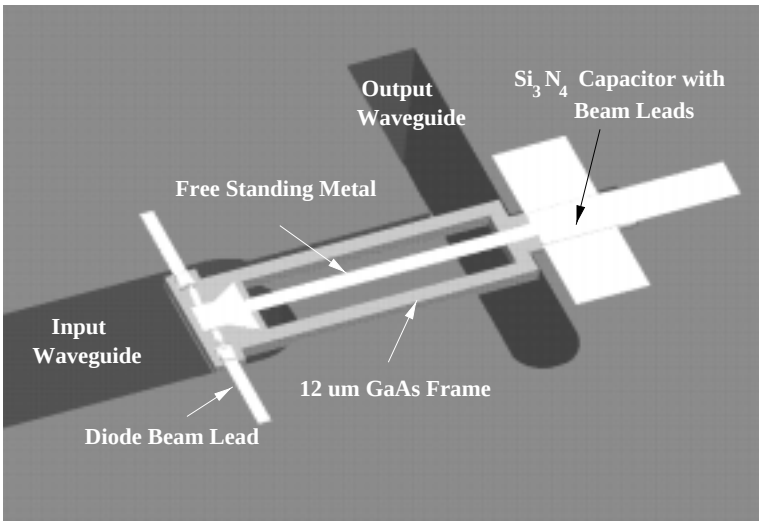

Fig. 1. Sketch of the 800 GHz doubler. The doubler chip rests on its beam leads on the split waveguide block.

II. Design, Fabrication and Assembly

The 800 GHz balanced doubler design process involves a few steps: Agilent Advanced Design System's (ADS) [3] nonlinear harmonic balance simulator is used to optimize the doping profile and diode dimensions like the anode and mesa size for a given input power (we used 7 mW input power for our design). From this simulation we also calculate the diode junction characteristics as a function of frequency and the embedding impedances for optimum performance of the multiplier. Then the multiplier input and output matching circuits are synthesized using Ansoft High Frequency Structure Simulator (HFSS) – a finite element electromagnetic simulator [4]. Using the S-parameters obtained from HFSS simulations, and the diode properties obtained from the nonlinear diode simulations, we optimize the design in a linear simulator with waveguide matching components for maximum doubler efficiency. As a final step, we put all the design elements in the nonlinear harmonic balance simulator which predicts the simulated performance of the doubler.

The input signal is directly coupled to the diodes which are placed in a reduced height input waveguide. The output signal is coupled to the output waveguide by means of a E-field probe. The input matching is accomplished with the input backshort and waveguide matching sections, and the output circuit is optimized using waveguide matching components, a waveguide channel connecting the input and output waveguides, and a small open stub on the input side of the diode which tunes out the inductance of the diode structure at the output frequency. An integrated Si_3N_4 metal insulator metal (MIM) capacitor, at the end of output coupling probe, is used as RF short and DC bypass. One of the critical design criteria is to make the input reduced height section below cut-off for TM_{11} mode at the output frequency. The cavity for the MIM capacitor should also be designed carefully not to allow any output frequency signal leak through it. Fig. 1 shows the designed doubler chip placed inside the split waveguide block. The expected performance from the doubler is shown in Fig. 2.

The device and circuitry for the doubler is fabricated on a Gallium Arsenide (GaAs) substrate using optical lithography and conventional epitaxial layers [5]. The doping used for these devices is $4 \times 10^{17}/\mathrm{cm}^3$. What is unique about this fabrication process is the use of metal beam leads for DC and RF contacts with waveguides. Also, to minimize dielectric loading of the waveguides and to reduce RF losses in passive circuits, GaAs substrate under the transmission lines is removed in back-side processing, leaving free standing metal lines suspended in air from 12 μm thick GaAs frame. Fig. 3 shows the picture of the devices fabricated. Fig. 3(a) shows the nominal device with the picture inset showing the close-up of the diode area. We have a

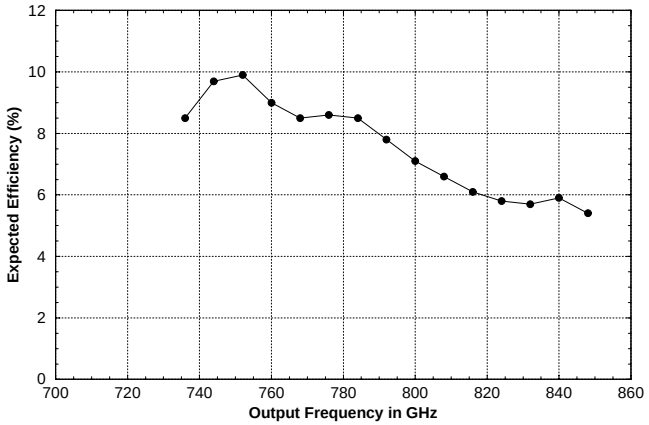

Fig. 2. Expected simulated performance from the 800 GHz doubler. The device used for this simulation is 1.1 μm $\times$ 1.0 μm diode on a $4 \times 10^{17}/\text{cm}^3$ doped substrate. 7 mW of input pump power was used for simulation.

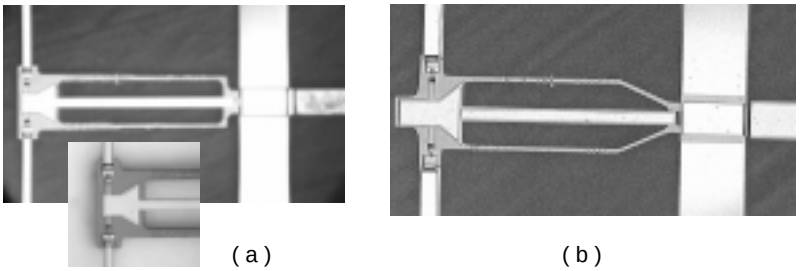

Fig. 3. Picture of the fabricated devices: (a) nominal design, with the picture inset showing close-up of the diode area, (b) a design variation which has a different frame structure.

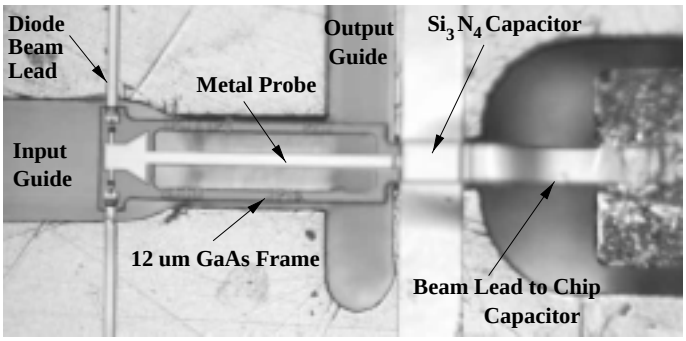

Fig. 4. Picture of the assembled 800 GHz doubler. The anode size for the diode is 1.1 μm $\times$ 1.0 μm, and has $4 \times 10^{17}/\text{cm}^3$ substrate doping.

few design variations on the wafer, and Fig. 3(b) shows such a variation where the frame is designed differently and the tuning stub is a bit longer. We also have a few anode size variations for the design on the wafer.

Assembly for this device is relatively simple, fast, and robust. The diode chip is dropped inside the split waveguide block with the diode beam leads resting on the waveguide metal. The beam lead from the MIM capacitor is bonded to a chip capacitor which in turn is wire-bonded to the bias connector. There is no soldering or other high temperature procedure used on the device and that reduces the possibility of device damage. The assembled doubler picture is shown in Fig. 4.

III. Measurement and Results

The generic scheme we use for power and frequency measurement is shown in Fig. 5. A pump source, either a BWO, or a Gunn oscillator, or a frequency synthesizer along with a multiplier, generates a signal in the 90–110 GHz frequency range. Since we need about 7–10 mW of input power at 400 GHz to pump our 800 GHz doubler, the 100 GHz signal source needs to be amplified and power combined to generate about 200 mW of input power, as shown in Fig. 5. We use our 200 GHz and 400 GHz doublers [1] to generate the pump signal for the 800 GHz doubler. Initial measurements are carried out at room temperature using a wideband calorimeter [6]. The picture of our room temperature measurement setup on the bench is shown in Fig. 6. The multiplier chain is then placed in a cryostat where power is measured quasi-optically using a Thomas Keating power meter [7]. The cryostat is used for measurements both at room temperature and at cryogenic temperatures.

The performance of the doubler at room temperature is shown in Fig. 7. The figure inset shows the input power used to pump the 800 GHz doubler. The result shown does not correct for any window loss at the cryostat or any other losses in the circuit, the waveguide, or the external components. We measured more than 10% efficiency at 770 GHz, giving about 1.1 mW of peak output power at room temperature when pumped with about 9 mW of input power. Output power at high frequency end drops to about 200 μW range because of non availability of sufficient pump power. The output power curve more or less follows the input power plot.

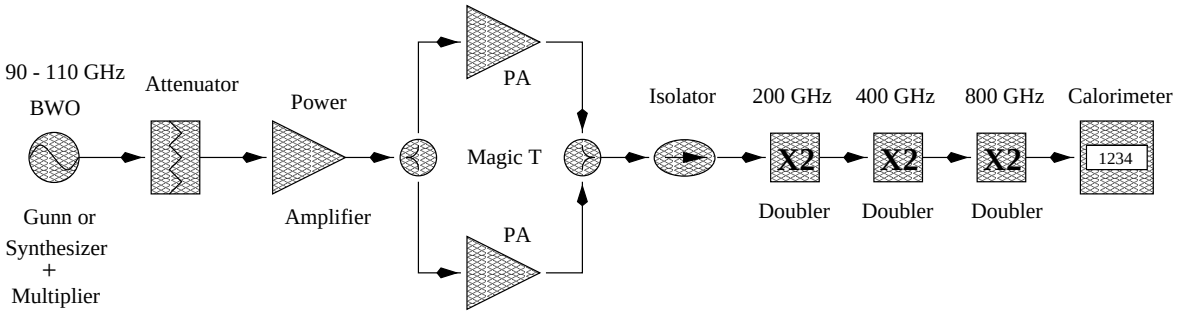

Fig. 5. Schematic of the generic measurement setup for power and frequency measurement.

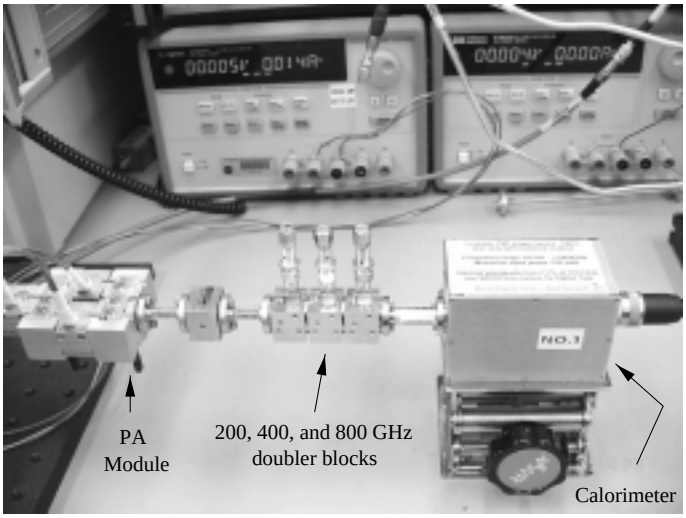

Fig. 6. Picture of the 800 GHz doubler measurement setup.

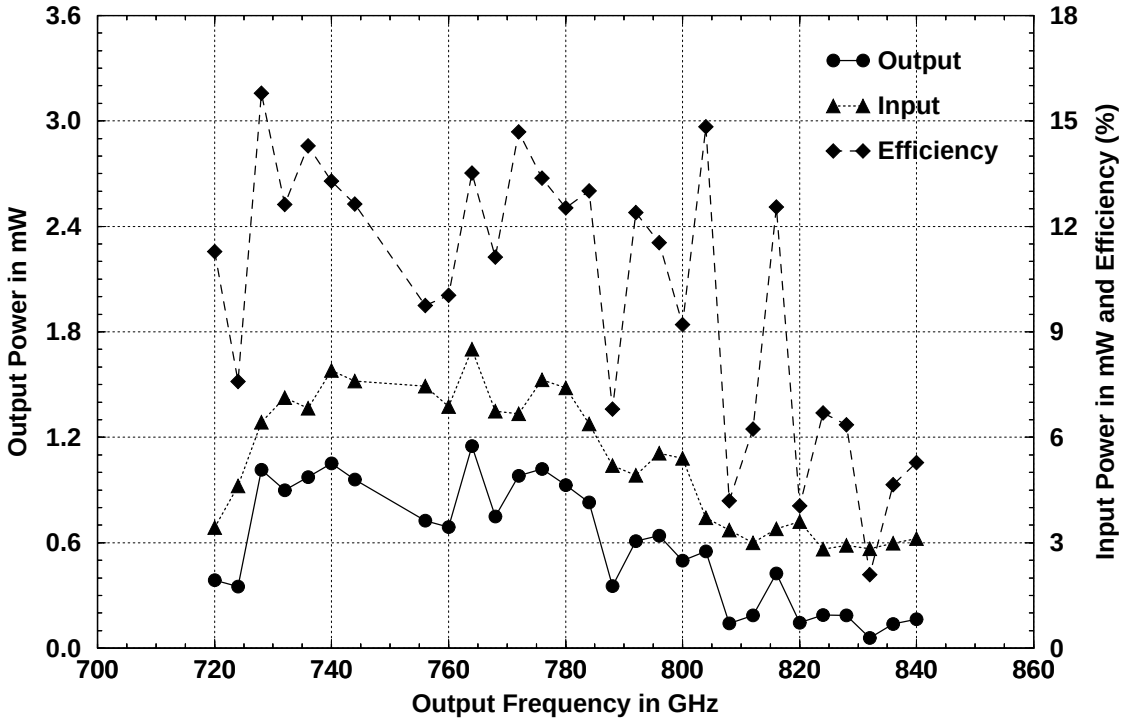

Fig. 7. Performance of the doubler at room temperature. The anode size used for the doubler is 1.1 μm $\times$ 1.0 μm .and has $4 \times 10^{17}/\text{cm}^3$ substrate doping. The firm line with the circles shows the output power in mW, the dotted line with the triangles shows the input power used to pump the doubler and the dashed line with the diamonds shows the efficiency plot.

We wanted to measure the doubler at cryogenic temperatures as well, but there was an unfortunate mishap. While tuning the bias voltage for room temperature measurement, the doubler was biased too close to the breakdown voltage of the diodes, damaging the device in the process. The diode I-V plot was found to be much softer after this, and we measured about 930 μW of output power at 770 GHz instead of 1.1 mW which was measured earlier at room temperature. We cooled this damaged device anyway, and measured about 1.1 mW of output power at the same frequency at 120 K temperature, an improvement of about 20%. Since the entire chain, except for the power amplifiers, was cooled, we expected better performance at 120 K. However, the device was damaged, and we suspect that's the reason for not getting expected improvement from the doubler at cryogenic temperatures. We are assembling another doubler and expect to get better results when cryogenically cooled.

IV. Conclusion

We have designed and evaluated a wide band fixed tuned 800 GHz balanced frequency doubler. This balanced doubler achieved more than 10% efficiency at 770 GHz, giving about 1.1 mW peak output power when pumped with 9.0 mW of input power. This represents the best performance from any doubler at these frequencies to date in literature. We also measured the doubler at cryogenic temperatures, and found about 20% improvement in output power when cooled to 120 K temperature. In future, we plan to test all the different design variations that have been fabricated, and also want to evaluate the performance at cryogenic temperatures more carefully. We have a few devices fabricated on $2 \times 10^{17}/\text{cm}^3$ doped substrate, and we want to test them as well. The reason for fabricating devices with $2 \times 10^{17}/\text{cm}^3$ doping is that we expect better performance from these devices when cooled to 120 K. We also to want to use the doubler as a driver stage to pump our high frequency doubler (1600 GHz) and tripler (2400 GHz) stages.

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