

Development of a Two-Pixel Integrated Heterodyne Schottky Diode Receiver at 183GHz

Hui Wang^{1,*}, Alain Maestrini¹, Bertrand Thomas², Byron Alderman² and Gérard Beaudin¹

¹Observatoire de Paris, LERMA, 61 Avenue de l'Observatoire, 75014 Paris, France

²Rutherford Appleton Laboratory, STFC, Chilton Didcot, OX11 0QX, Oxfordshire, UK.

* Contact: hui.wang@obspm.fr, phone +33-1-40512079

Abstract— This paper describes the design of a two-pixel Schottky diode-based heterodyne receiver working at 183GHz. The receiver is the integration of two 183GHz subharmonic mixers and a frequency tripler into the same mechanical block. A Y junction divider is used to split the power produced by the frequency multiplier. The chips have been fabricated using the standard BES process of United Monolithic Semiconductors (UMS) in the frame of a contract with the Centre National d'Etudes Spatiales (CNES) and the European Space Agency (ESA). The integrated two-pixel receiver is expected to work in the band 170-195 GHz with a double side band (DSB) conversion gain greater than -5.5dB when pumped with less than 50mW of input power at 30GHz. A minimum DSB conversion gain of -4.5dB at 183 GHz is expected.

I. INTRODUCTION

In planetary and atmospheric sciences large arrays of millimeter wave heterodyne Schottky diode-based receivers can offer higher mapping speed and mapping consistency while avoiding the use of cryogenic receivers. To reduce the size, the weight and the power consumption of a multi-pixel receiver it is necessary to optimize the interface between the mixers and the local oscillator unit. One solution consists in integrating in the same mechanical block a frequency multiplier and one or several mixers to create a compact sub-array.

II. TWO-PIXEL INTEGRATED RECEIVER AT 183GHZ

A novel approach to design multi-pixel heterodyne receiver is described below. Based on this idea, we could extend the number of beams after changing the LO distribution network. This concept could be applied to higher frequencies.

A. Design Approach and Model

Large heterodyne arrays are possible only by higher levels of component integration with associated package and power dissipation issues [1]. The challenges in developing large arrays of heterodyne detectors relate to the mixer configuration, local oscillator (LO) power coupling, the intermediate frequency (IF) layout, and the back-end processing. In our configuration, one single solid state LO source pump two mixers simultaneously by using a power divider. In addition, the mixers and the frequency multiplier are integrated in a same waveguide block. Figure 1 shows the

topology of this two-pixel integrated receiver. Two IF signals are collected vertically with standard SMA connector. The mixer and the tripler chips were both optimized independently for two stand-alone circuits. The design of this mixer and this tripler are detailed respectively in section III and section IV.

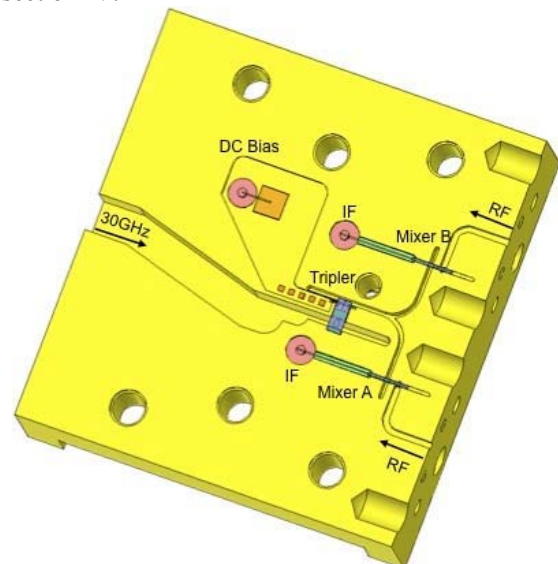


Fig. 26 Schematic of the bottom block of the two-pixel integrated receiver with the IF connector and DC bias.

B. Optimization and Simulation Result

We used the same mixer and tripler chips for the two-pixel integrated receiver as for the stand-alone 183 GHz mixer and 90 GHz tripler circuits. The optimization of the two-pixel receiver was performed by several steps. Firstly, the input waveguide back short, the input waveguide steps and the output waveguide back short of the tripler were re-optimized as a novel stand-alone tripler. Actually, to reduce the size of the integrated receiver, the height of the output waveguide of the tripler and the height of the LO waveguide of the mixers were reduced contrary to the stand-alone versions that had full height waveguides. Secondly, a reduced-height waveguide Y junction was optimized for splitting evenly the output power of the 90 GHz tripler. Thirdly, the RF waveguide back short, RF waveguide steps and the OL waveguide back short of the 183GHz mixers were re-

optimized. Finally, the optimization of the complete receiver was performed by tuning both the distance between the output probe of the tripler and the Y junction, and the distance between the LO waveguide of the mixer and the Y junction in order to get an optimum LO coupling. All the simulations and optimizations were performed by using Ansoft HFSS and Agilent ADS.

The predicted performance of the integrated receiver is presented in Figure 2. The two mixers have almost identical noise temperature. By tuning the input power of the receiver from 30mW to 100mW, the optimum performance of the receiver can be reached. A minimum DSB mixer noise temperature of 500K at 183GHz is expected for the two mixers with an input power of 50mW at 30GHz.

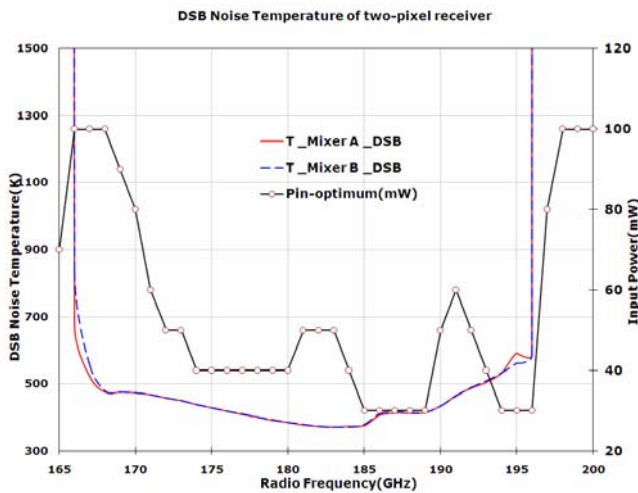


Fig. 27 The bottom solid line and the dashed line show respectively the simulated DSB mixer noise temperature for two pixels with optimum input power; the plain curves with open marker show the optimum input power to the receiver.

III. 183GHZ MMIC SHP2 MIXER

The 183GHz MMIC subharmonic mixer was optimized independently for a stand-alone circuit.

A. Mixer Layout

This is a broadband fixed-tuned 183 GHz sub-harmonically pumped mixer featuring an anti-par -8allel pair of planar Schottky diodes monolithically integrated on a 50 μm -thick GaAs substrate. The circuit was fabricated using the standard BES process of United Monolithic Semiconductors (UMS). The circuit is about 4 mm long, 0.28 mm wide and is mounted in a waveguide split block that includes waveguide matching elements at the Local Oscillator (LO) and RF frequencies (Figure 3). Design details are described in [2].

The mixer is expected to work efficiently in the band 160-190 GHz using only 2mW of LO pump power, with a Double Side Band (DSB) conversion gain greater than -5.5 dB. The best performance obtained in simulations is a DSB gain of -5.1 dB at 183 GHz.

Unfortunately, due to misalignments during the steps processing, the mixer chip presents unbalanced diodes with series resistances of 21 Ω and 12.5 Ω .

B. Measurements

For the experiments, the LO fundamental source was provided by a 8-18GHz Yig oscillator from an AB Millimetre Network Vector Analyzer, which as used to drive a commercial sextupler followed by a power amplifier both from Radiometer Physics GmbH; this LO source chain could provide about 10mW from 75GHz to 100GHz. This source chain was calibrated with an Erickson power meter [3]. A W band waveguide attenuator was used to adjust the pump power for the mixer. A directional coupler inserted before the mixer measured the pump power coupled into the mixer.

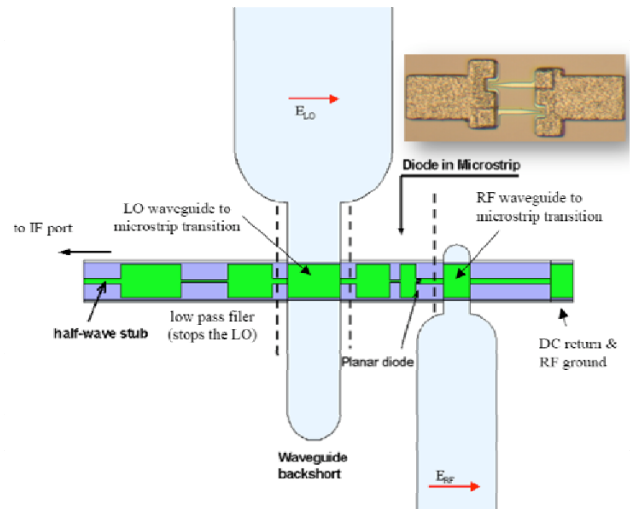


Fig. 28 Schematic of the MMIC mixer circuit and waveguide matching elements, an anti-parallel pair of diodes is shown on the top right.

We use a 2-4GHz IF chain that includes a low-loss isolator at its input and an internal noise source that can be switched ON and OFF to modify the noise factor of the IF chain. The noise temperature of the IF chain is 194.4K when the internal noise source is ON, and 81.2K when the noise source is OFF.

The equivalent noise temperature of the receiver was measured by presenting alternatively a room temperature and a liquid nitrogen-cooled blackbody in front of the mixer feedhorn. Two independent receiver equivalent noise temperature measurements are performed: one with the internal noise source ON the other with the internal noise source OFF. We use the classic Y-factor method to calculate the receiver noise temperature. The Y factor was measured with an Agilent E9325A (0.05-18GHz) power sensor corrected from its non-linearity in a separate calibration procedure. This test bench can achieve an accuracy of 0.001dB for the Y factor measurement.

All the measurements were performed at room temperature. Mixer DSB noise temperatures, mixer conversion losses and the LO pump powers as a function of RF frequency are presented below in Figure 4&5. The measured noise temperatures and conversion losses are significantly higher than the predicted values. This could be partly due to the unbalance of the diodes. Preliminary simulations have been performed with unbalanced diodes,

showing that the difference on the mixer noise temperature is only of about 100K. The optimum pump power in the band 160-190GHz is however in very good agreement with simulation results.

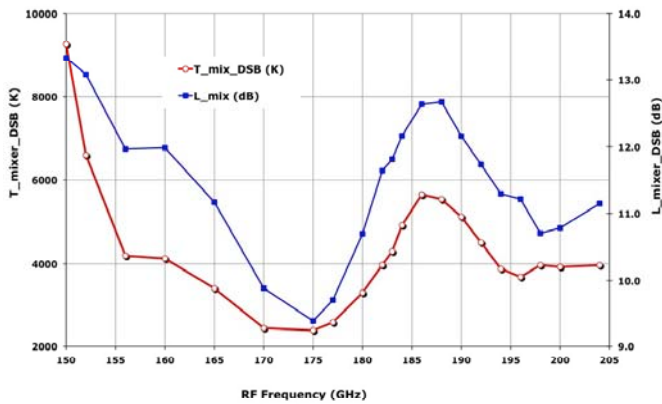


Fig. 29 The top plain curve with filled square markers and the bottom plain curve with open circles show respectively the measured DSB mixer noise temperature and the measure DSB mixer conversion losses.

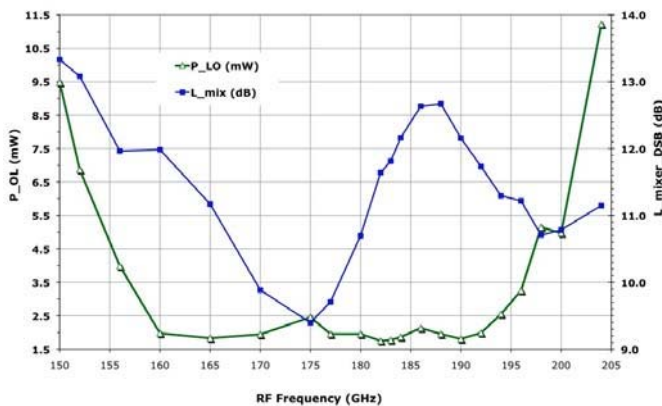


Fig. 30 The top plain curve with filled square markets shows the measure DSB mixer conversion losses, the bottom plain curve with open circles show the LO pump power.

IV. 90GHZ MMIC FREQUENCY TRIPLER

A. Design

A 6-anode balanced tripler was designed based on the same topology shown in [4]. The tripler uses the so-called open-loop configuration that allows more than two diodes to be easily implanted on chip dramatically increasing the power handling capabilities of the multiplier.

1) Topology and optimization

In our design, this loop is created by 6 diodes that are in series at DC but appear to be in an anti-parallel configuration at the RF, due to the symmetry of the excitation and the symmetry of the circuit. This virtual loop can only work if the suspended microstrip line that the diodes are connected to cannot propagate the parasitic (TE) mode at the second harmonic.

The matching of the diode is performed both by a succession of high and low impedance sections printed on

chip and by the input and the output probes with their respective back-shorts. To widen the bandwidth, the circuit features additional matching elements in the input and output waveguides, made with a succession of waveguide sections of different heights and lengths.

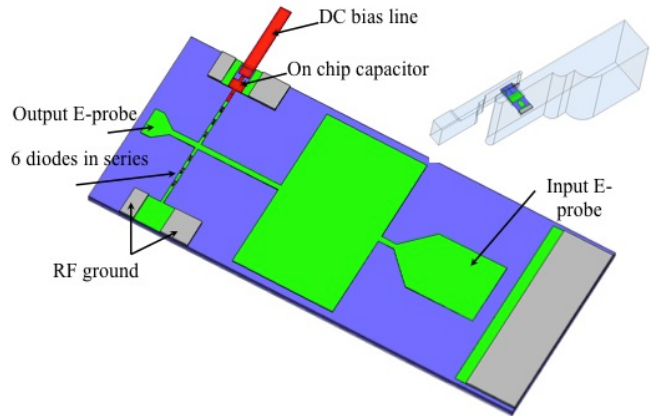


Fig. 31 Schematic of tripler chip on GaAs substrate without channel and waveguides and the top right corner shows the hip inside waveguide.

Special attention was put on the biasing scheme, which is usually tricky for high frequency circuits. UMS BES process provides on-chip capacitors: that can be small enough to fit on the multiplier chip. The RF grounding to the block will be made by silver epoxy glue; the DC line will be connected to the on-chip-capacitor via a wire-bond.

The optimization is performed using Ansoft HFSS and Agilent ADS. The optimization method was presented in [5].

2) Tripler architecture and fabrication

The chip features six Schottky diodes using UMS BES process with wide gate width ($>10\mu\text{m}$), each anode has the following characteristics: an ideality factor $\eta = 1.2$, saturation current $I_{\text{SAT}} = 4.10\text{-}15\text{A}$, series resistance $R_s = 5\ \Omega$, the optimum junction capacitance $C_j = 36\ \text{fF}$ (optimized) and the length of anode $22\ \mu\text{m}$ (gate width). The 6 diodes are connected in series and integrated on a $1360\ \mu\text{m}$ wide substrate, suspended in a channel with the width of channel of $1400\ \mu\text{m}$ and the height of channel of $550\ \mu\text{m}$ (Figure 6). Figure 7 shows a wafer photograph of the tripler chip.

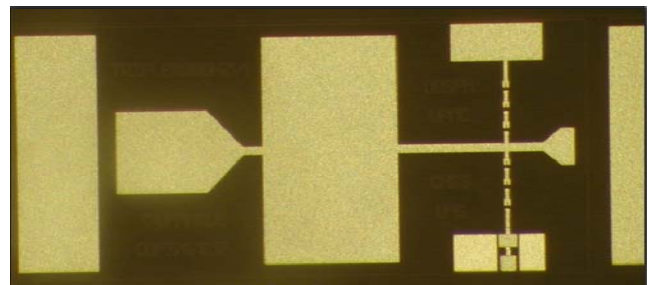


Fig. 32 On wafer photograph of the tripler.

B. Simulation Result

The predicted performance of the tripler is presented in Figure 8. The average efficiency from 29- 32GHz is about

13% and corresponds to the output powers of about 6.5mW, which is sufficient to pump the subharmonic mixer. These estimated efficiencies are for 50mW of input power.

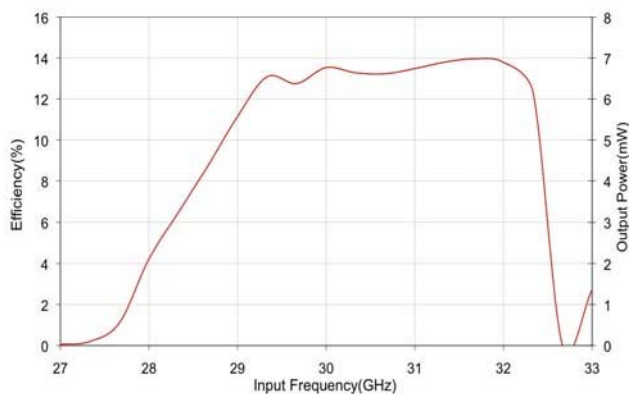


Fig. 33 Predicted efficiency and output power VS input frequency for an input power of 50 mW.

CONCLUSIONS

A novel topology of integrated heterodyne detector working at room temperature has been proposed. It is believed that this design is suitable to create larger arrays of heterodyne detectors and apply for higher frequencies. The circuits have been fabricated using the standard BES process of United Monolithic Semiconductors (UMS). The measurement of the 90GHz tripler and the machining of the two-pixel receiver will be accomplished during the summer of 2008. The test of the complete receiver would be performed later this year.

ACKNOWLEDGMENT

The authors wish to thank the Precision Development Facility at RAL for the machining of the mixer and tripler block and the support from CNES, the Centre National Recherche Scientifique (CNRS), AB Millimetre in France, ESA and the Rutherford Appleton Laboratory in the United Kingdom.

REFERENCES

- [1] G. Chattopadhyay, I.Mehdi, J. S. Ward, E.Schlecht, A. Skalare, and P. H. Siegel, "Development of Multi-pixel Heterodyne Array Instruments at Submillimeter Wavelengths," *Proceedings of the Asia Pacific Microwave Conference*, New Delhi, India, December 2004.
- [2] H. Wang, J.-M. Rollin, B. Thomas, S. Davies, B. Alderman and A. Maestrini, "Design of a low noise integrated sub-harmonic mixer at 183 GHz using European Schottky diode technology," in *Proceedings of the 4th ESA workshop on Millimetre-Wave Technology and Applications*, Espoo, Finland, February 2006, pp.249-252, .
- [3] N. R. Erickson, "A fast and sensitive submillimeter waveguide power sensor," in *Proc. 10th Int. Symp. Space Terahertz Technology*, Charlottesville, VA, 1999, pp. 501-507.
- [4] A. Maestrini, Charlotte Tripon-Canseliet, John S. Ward, John J. Gill, Hamid H. S. Javadi, Erich Schlecht, Goutam Chattopadhyay, and Imran Mehdi, "Multiple-Anode Broadband Frequency Triplers at Submillimeter Wavelengths," in *Proc. 16th Int. Symp. Space Terahertz Technology*, Göteborg, Sweden, May 2005.
- [5] A. Maestrini, John S. Ward, John J. Gill, Hamid H. S. Javadi, Erich Schlecht, Charlotte Tripon-Canseliet, Goutam Chattopadhyay, and Imran Mehdi, "A 540-640 GHz High Efficiency Four Anode Frequency Tripler," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 9, pp. 2835-2843, Sep. 2005.